STIC Search Report
EIC 2100

STIC Database Tracking Number: 123943

TO:	From:
Chongshan Chen **Location: 4B25** **Art Unit: 2172** **Wednesday, June 09, 2004** **Case Serial Number: 09/842370**	**Anne Hendrickson** **Location: EIC 2100** **PK2-4B40** **Phone: 308-7831** **Anne.Hendrickson@uspto.gov**

Search Notes

Jason - Attached is the NPL search for the above referenced case. I have tagged references that I thought might be of interest. After taking a look at the results, please let me know if you would like for me to refocus the search in any way. I'd be happy to do so.

Anne

STIC EIC 2100 123943
Search Request Form 32

Today's Date: 6/7/04

What date would you like to use to limit the search?
Priority Date: 4/25/2000 Other:

Name Chongshan Chen
AU 2172 Examiner # 79547
Room # 4B25 Phone 305-8319
Serial # 09/842,370

Format for Search Results (Circle One):
(PAPER) DISK EMAIL

Where have you searched so far?
(USP) DWPI EPO JPO ACM IBM TDB
IEEE INSPEC SPI Other _____

Is this a "Fast & Focused" Search Request? (Circle One) YES (NO)
A "Fast & Focused" Search is completed in 2-3 hours (maximum). The search must be on a very specific topic and meet certain criteria. The criteria are posted in EIC2100 and on the EIC2100 NPL Web Page at http://ptoweb/patents/stic/stic-tc2100.htm.

What is the topic, novelty, motivation, utility, or other specific details defining the desired focus of this search? Please include the concepts, synonyms, keywords, acronyms, definitions, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract, background, brief summary, pertinent claims and any citations of relevant art you have found.

An apparatus for manging data corresponding to a plurality of reticles in a semiconductor manufacturing system comprising:

a central reticle database configured and arranged to store data associated with the plurality of reticles;

a stocker including a stocker database, a stocker controller communicably coupled to the stocker database, the stocker controller being configured and arranged to store at least a portion of the data corresponding to the at least one of the plurality of reticles stored within the plurality of storage locations within the stocker database.

STIC Searcher _____ Phone _____
Date picked up _____ Date Completed _____

Search and Information Resources Administration

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?ds

Set     Items   Description
S1     392118   RETICLE? OR MASK? OR PHOTOMASK? OR WAFER? OR RETICULE?
S2    2601408   STOCK? OR STORAGE? OR INVENTORY? OR INVENTORI? OR WAREHOUS?
             OR SUPPLY? OR SUPPLIE???
S3    1264482   SEMICONDUCTOR? OR INTEGRATED()CIRCUIT? OR IC OR ICS
S4     205139   DATABASE? OR DATA()BASE? OR DB OR DBS OR DBMS OR MANAGEMEN-
            T()SYSTEM? OR DATABANK? OR DATA()BANK? ? OR DATAFILE? ? OR DA-
            TA()FILE? ? OR DATA()MANAG?
S5        181   S1 AND S2 AND S3 AND S4
S6         62   S5 AND IC=G06F?
S7     140595   (CENTRAL? OR MASTER OR MAIN OR PARENT OR PRIMARY OR CONSOL-
            IDAT? OR HOST?)(2W)(DATABASE? OR DATA()BASE? OR ARCHIVE? OR R-
            EPOSITOR? OR LIBRAR?? OR AUTHORITY OR SERVER? ? OR NODE? ? OR
            COMPUTER? ? OR TERMINAL? ? OR DIRECTOR? OR SITE OR HO...
S8          4   S6 AND S7
S9          7   S6 AND CONTROLLER?
S10         7   S9 NOT S8
?show files
File 350:Derwent WPIX 1963-2004/UD,UM &UP=200435
         (c) 2004  Thomson Derwent
File 347:JAPIO Nov 1976-2004/Jan(Updated 040506)
         (c) 2004 JPO & JAPIO
?
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?t s8/5/2,3,4

8/5/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2004 Thomson Derwent. All rts. reserv.

015142791 **Image available**
WPI Acc No: 2003-203318/200320
XRPX Acc No: N03-161993
Information management system **and method, for a networked** semiconductor **manufacturing system, that uses a decryption key to protect manufacturing data**
Patent Assignee: CANON KK (CANO); NAKAMURA T (NAKA-I)
Inventor: NAKAMURA T
Number of Countries: 032 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 1282065	A1	20030205	EP 2002255311	A	20020730	200320 B
US 20030028486	A1	20030206	US 2002202909	A	20020726	200320
JP 2003046496	A	20030214	JP 2001232760	A	20010731	200322

Priority Applications (No Type Date): JP 2001232760 A 20010731
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 1282065	A1	E	16	G06K-001/12	
US 20030028486	A1			G06F-017/60	
JP 2003046496	A		8	H04L-009/10	

Designated States (Regional): AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI SK TR

Abstract (Basic): EP 1282065 A1
NOVELTY - Encrypted **semiconductor** manufacturing data is transmitted from a networked **host computer** (1) to an exposure device (2). Decryption key data and **mask** identification information is also sent from the **host** to a **mask stocker** (10). The exposure device decrypts the encrypted manufacturing data in accordance with the decryption key data which is prerecorded on the **mask** .
USE - For a networked **semiconductor** manufacturing system.
ADVANTAGE - Prevents unauthorized access, via the network, to sensitive manufacturing data.
DESCRIPTION OF DRAWING(S) - The figure shows a view of the networked **semiconductor** manufacturing system.
pp; 16 DwgNo 1/4
Title Terms: INFORMATION; MANAGEMENT; SYSTEM; METHOD; **SEMICONDUCTOR** ; MANUFACTURE; SYSTEM; DECRYPTER; KEY; PROTECT; MANUFACTURE; DATA
Derwent Class: T01
International Patent Class (Main): **G06F-017/60** ; G06K-001/12; H04L-009/10
International Patent Class (Additional): G09C-001/00; H01L-021/02; H01L-021/027; H04L-009/32
File Segment: EPI

8/5/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2004 Thomson Derwent. All rts. reserv.

010068717 **Image available**
WPI Acc No: 1994-336430/199442
XRPX Acc No: N94-264309
Production management system semiconductor wafer **- has** host computer **which memorises** semiconductor wafer , **processing progress situation,** stock **situation based on bar code label information on each cassette accommodating** wafer **NoAbstract**
Patent Assignee: MITSUBISHI MATERIAL SILICON KK (MITV); MITSUBISHI MATERIALS CORP (MITV)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 6260545	A	19940916	JP 9342431	A	19930303	199442	B

Priority Applications (No Type Date): JP 9342431 A 19930303
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 6260545	A		15	H01L-021/68	

Abstract (Basic): JP 6260545 A
Dwg.1/10
Title Terms: PRODUCE; MANAGEMENT; SYSTEM; **SEMICONDUCTOR** ; **WAFER** ; **HOST** ; COMPUTER; MEMORY; **SEMICONDUCTOR** ; **WAFER** ; PROCESS; PROGRESS; SITUATE; **STOCK** ; SITUATE; BASED; BAR; CODE; LABEL; INFORMATION; CASSETTE; ACCOMMODATE; **WAFER** ; NOABSTRACT
Derwent Class: P62; U11
International Patent Class (Main): H01L-021/68
International Patent Class (Additional): B25J-015/08; **G06F-015/21** ; H01L-021/02
File Segment: EPI; EngPI

8/5/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010000038 **Image available**
WPI Acc No: 1994-267749/199433
XRPX Acc No: N94-210951
Prodn process management system **for** semiconductor **industry which does not cause trouble to conveyance system - uses separate process, movement programs and independent** stock **control to carry out routine**
Patent Assignee: MITSUBISHI ELECTRIC CORP (MITQ)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 6196544	A	19940715	JP 92346444	A	19921225	199433	B

Priority Applications (No Type Date): JP 92346444 A 19921225
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 6196544	A		7	H01L-021/68	

Abstract (Basic): JP 6196544 A
The process **management system** has an array of **host** and slave stations. The **semiconductor wafers** are arranged in a predetermined manner in the **stockers** (12). The **stocker** control module (4) controls the movement of the **stocker** and receives address of next **stocker** movement from **IC** card (11), and through control part (3) feeds the same to **stocker** .
The **IC** card is connected to lot case (6). A **stocker** management terminal (9) is provided in **stocker** control and this is used to read and write data from and into **IC** card. The process and movement management are computed simultaneously.
USE/ADVANTAGE - Controls **storage** , conveyance, etc. of **wafer** used in **semiconductor** prodn. Increases efficiency of systems and carries out two independent routines. Performs production process management even when the **host** system breaks down. Controls migration between **stockers** of a lot case.
Dwg.1/5
Title Terms: PRODUCE; PROCESS; MANAGEMENT; SYSTEM; **SEMICONDUCTOR** ; INDUSTRIAL; CAUSE; TROUBLE; CONVEY; SYSTEM; SEPARATE; PROCESS; MOVEMENT; PROGRAM; INDEPENDENT; **STOCK** ; CONTROL; CARRY; ROUTINE
Derwent Class: Q35; U11
International Patent Class (Main): H01L-021/68
International Patent Class (Additional): B65G-037/02; B65G-049/07; **G06F-015/21** ; H01L-021/02
File Segment: EPI; EngPI

?t s10/5/1,2,4

10/5/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015910603 **Image available**
WPI Acc No: 2004-068443/200407
XRPX Acc No: N04-055048
Material transfer request management method for semiconductor **fabrication, involves passing request from factory to material handling system, by comparing number of material backlogged in designated target with threshold**
Patent Assignee: ADVANCED MICRO DEVICES INC (ADMI)
Inventor: CONBOY M R; GROVER J; SHIRLEY R
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6662076	B1	20031209	US 99247659	A	19990210	200407	B

Priority Applications (No Type Date): US 99247659 A 19990210
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6662076	B1		12	G06F-007/00	

Abstract (Basic): US 6662076 B1
NOVELTY - A request to transfer a material to a designated target is transmitted from a factory system (110) to an automated material handling system (AMHS) (120). A broker (130) coupled to the system, compares the number of material backlogged in the target with threshold limit and selectively pass the requests based on comparison.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for material transfer request **management system** .
USE - For managing material such as **wafer** transfer request in fabrication of **semiconductor** .
ADVANTAGE - Since the material backlogged in target position is compared before passing the request, the log jams of material in the AMHS is reduced, and thereby increasing the ease of operation.
DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of the transfer request managing system.
factory system (110)
automated material handling system (120)
storage tool **controller** (122)
equipment interface (126)
broker (130)
pp; 12 DwgNo 1/6
Title Terms: MATERIAL; TRANSFER; REQUEST; MANAGEMENT; METHOD; **SEMICONDUCTOR** ; FABRICATE; PASS; REQUEST; FACTORY; MATERIAL; HANDLE; SYSTEM; COMPARE; NUMBER; MATERIAL; DESIGNATED; TARGET; THRESHOLD
Derwent Class: T01; U11
International Patent Class (Main): **G06F-007/00**
File Segment: EPI

10/5/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015695117 **Image available**
WPI Acc No: 2003-757306/200371
XRAM Acc No: C03-207932
XRPX Acc No: N03-606852
Material supply **system for use in processing facilities of** semiconductor **device manufacturing plant comprises** controller **for controlling** supply **of material from source to processing facilities**
Patent Assignee: EBARA CORP (EBAR); TOSHIBA KK (TOKE)
Inventor: AKAHORI M; MIYAZAKI K; NADAHARA S; NAKAGAWA S; NAKAJIMA K; USUDA

K
Number of Countries: 004 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200381647	A1	20031002	WO 2003JP3874	A	20030327	200371	B
JP 2003282386	A	20031003	JP 200288153	A	20020327	200382	

Priority Applications (No Type Date): JP 200288153 A 20020327
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200381647	A1	E	73	H01L-021/02	
Designated States (National): CN KR US					
JP 2003282386	A		24	H01L-021/02	

Abstract (Basic): WO 200381647 A1
NOVELTY - A material **supply** system comprises a material **supply** source; and a **controller** for controlling material **supply** from a source to processing facilities such that a total amount of the material currently used by the processing facilities does not exceed an amount of the material which can be **supplied** from the source, by controlling a start timing from which the material is **supplied** to a processing facility.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a **semiconductor** device manufacturing plant having processing facilities and comprising a material **supply** system; a **database** for logging and managing processes in each of the processing facilities; and a computer-integrated manufacturing (CIM)-based control system for totally controlling the **semiconductor** device manufacturing plant, in which the control system sets a **supply** rate at which the material to the processing facilities, priorities for **supplying** the material among the processing facilities based on an operation schedule for the processing facilities and a **semiconductor** device manufacturing schedule on the **database** .
USE - Used for **supplying** the same kind of gas, liquid or solid material to processing facilities in a **semiconductor** device manufacturing plant (claimed).
ADVANTAGE - The system entails a low initial cost and running cost. it is capable of efficiently **supplying** processing facilities with just the required amounts of materials only when they are required for processing **semiconductor wafers** .
DESCRIPTION OF DRAWING(S) - The figure shows a material **supply** system for **supplying** a material to a polycrystalline or non-crystalline silicon film low pressure chemical vapor deposition equipment.
pp; 73 DwgNo 8/14
Title Terms: MATERIAL; **SUPPLY** ; SYSTEM; PROCESS; FACILITY; **SEMICONDUCTOR** ; DEVICE; MANUFACTURE; PLANT; COMPRISE; CONTROL; CONTROL; **SUPPLY** ; MATERIAL; SOURCE; PROCESS; FACILITY
Derwent Class: L03; T01; U11
International Patent Class (Main): H01L-021/02
International Patent Class (Additional): C02F-001/00; **G06F-017/60** ; H01L-021/304
File Segment: CPI; EPI

10/5/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011981666 **Image available**
WPI Acc No: 1998-398576/199834
XRPX Acc No: N98-310133
Database **management method for** semiconductor **device manufacturing plant - involves transmitting read data through polling engine to** database **system from which data is** supplied **to several programmable work stations**
Patent Assignee: TAIWAN SEMICONDUCTOR MFG CO LTD (TASE-N)

Inventor: LIN C
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5778386	A	19980707	US 96654365	A	19960528	199834	B

Priority Applications (No Type Date): US 96654365 A 19960528
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5778386	A		21	G06F-017/30	

Abstract (Basic): US 5778386 A

The method involves controlling a manufacturing operation using a **database** system. The manufacturing operation is configured to perform a specific task at each work station. A rack holds several pods that holds a **wafer** cassette. A tag is attached to each pod.

A **storage controller** is provided with the rack. Data for lots of work located in containers in the plant is read. The read data are transmitted through a polling engine and stored in a **database** system. The collected data is **supplied** from the **database** system to several programmable work stations that are connected by a star network to the **database** .

ADVANTAGE - Enables to perform function of different functional location by reconfiguring programmable workstation. Provides colourful graphical user interface.

1A,1B/13

Title Terms: **DATABASE** ; MANAGEMENT; METHOD; **SEMICONDUCTOR** ; DEVICE; MANUFACTURE; PLANT; TRANSMIT; READ; DATA; THROUGH; POLL; ENGINE; **DATABASE** ; SYSTEM; DATA; **SUPPLY** ; PROGRAM; WORK; STATION
Derwent Class: T01
International Patent Class (Main): **G06F-017/30**
File Segment: EPI
?

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?ds

Set     Items   Description
S1     392118   RETICLE? OR MASK? OR PHOTOMASK? OR WAFER? OR RETICULE?
S2    1751250   STOCKER? OR STORAGE? OR STORE? ? OR STORING OR INVENTORY? -
            OR INVENTORI? OR WAREHOUS?
S3    1264482   SEMICONDUCTOR? OR INTEGRATED()CIRCUIT? OR IC OR ICS
S4     205146   DATABASE? OR DATA()BASE? OR DB OR DBS OR DBMS OR MANAGEMEN-
            T()SYSTEM? OR DATABANK? OR DATA()BANK? OR DATAFILE? OR DATA()-
            FILE? OR DATA()MANAG?
S5        310   S1 AND S2 AND S3 AND S4
S6        121   S5 AND IC=G06F?
S7        401   S1(5N)S4
S8      51010   S2(5N)S4
S9         37   S6 AND S7 AND S3
S10        37   S9 AND IC=G06F?
S11         4   S6 AND (MC=T01-J05A2B OR T01-J07B)
S12        47   S7 AND S8 AND S3
S13        27   S12 NOT (S11 OR S10)
S14         0   S13 AND IC=G06F?
?show files
File 347:JAPIO Nov 1976-2004/Jan(Updated 040506)
      (c) 2004 JPO & JAPIO
File 350:Derwent WPIX 1963-2004/UD,UM &UP=200435
      (c) 2004  Thomson Derwent
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?t s10/5/6,7,10,13,15,17,18,19,20,21,22,26,28,29,30,31,32,34,37

10/5/6 (Item 6 from file: 347)
DIALOG(R)File 347:JAPIO

04089686 **Image available**
SEMICONDUCTOR SIMULATION DEVICE

PUB. NO.: 05-081386 [JP 5081386 A]
PUBLISHED: April 02, 1993 (19930402)
INVENTOR(s): TATSUMI TAKAAKI
APPLICANT(s): SONY CORP [000218] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 03-270242 [JP 91270242]
FILED: September 20, 1991 (19910920)
INTL CLASS: [5] **G06F-015/60** ; **G06F-015/20** ; H01L-021/82
JAPIO CLASS: 45.4 (INFORMATION PROCESSING -- Computer Applications); 42.2 (ELECTRONICS -- Solid State Components)
JAPIO KEYWORD: R011 (LIQUID CRYSTALS)
JOURNAL: Section: P, Section No. 1586, Vol. 17, No. 422, Pg. 41, August 05, 1993 (19930805)

ABSTRACT

PURPOSE: To prevent **mask** data and process data from being used by an inconsistent combination, and also, to execute rewriting and use of either one of them.

CONSTITUTION: The device is provided with a **mask data base** 14 for **storing mask** data, a process **data base** 10 for **storing** process data, a pair **data base** 6 for **storing** pair data for showing a pair of **mask** data and process data, and moreover, provided with a pair handling module 4 for rewriting the **storage** contents of the pair **data base** 6 in accordance with an editing request (for instance, contents change, deletion, copy, change of name, etc.), to at least one of the **mask** data and the process data.

10/5/7 (Item 7 from file: 347)
DIALOG(R)File 347:JAPIO

03903567 **Image available**
PRODUCTION **MANAGEMENT SYSTEM**

PUB. NO.: 04-268667 [JP 4268667 A]
PUBLISHED: September 24, 1992 (19920924)
INVENTOR(s): UCHIDA HIDEKI
OKAZAKI MAKOTO
FUJISHIRO TOMOHIRO
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 03-029826 [JP 9129826]
FILED: February 25, 1991 (19910225)
INTL CLASS: [5] **G06F-015/21** ; B23Q-041/08; G05B-015/02; H01L-021/02
JAPIO CLASS: 45.4 (INFORMATION PROCESSING -- Computer Applications); 22.3 (MACHINERY -- Control & Regulation); 25.2 (MACHINE TOOLS -- Cutting & Grinding); 26.9 (TRANSPORTATION -- Other); 42.2 (ELECTRONICS -- Solid State Components)
JOURNAL: Section: P, Section No. 1481, Vol. 17, No. 58, Pg. 121, February 04, 1993 (19930204)

ABSTRACT

PURPOSE: To automatically indicate supply in accordance with the fluctuation of the number of completed products by gathering production actual result information of each process and using this information for supply indication of parts, materials, or jigs with respect to a production

line where the quantity of products is varied in accordance with the advance of processes.

CONSTITUTION: An automatic **warehouse** 60 on a **semiconductor** production line preserves and supplies **masks** . An information processor 50 manages stocking and discharging of the automatic **warehouse** 60. A production actual result information input terminal 31 or the like is installed in each of processes 21, etc., and information processors 30, 31, etc., are connected by a transmission line 11. A form **mask DB** 41, a process **DB** 42, a **mask DB** 43, and a commencement **DB** 44 are generated on a central information processing unit 30. A worker inputs production actual result information at the time of carrying a **wafer** from an arbitrary process to the just succeeding process. The central information processing unit 30 refers to the process **DB** 42 to update the commencement **DB** 44 based on received information. Thus, **mask** supply indicating information is generated and is transmitted to an automatic **warehouse** control terminal 50.

10/5/10 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

016215456
WPI Acc No: 2004-373344/200435
Related WPI Acc No: 2004-316232; 2004-339416
XRAM Acc No: C04-140439
XRPX Acc No: N04-296917

Determining uniformity metrics of semiconductor wafer **manufacturing process, by scaling collected quantity data across first** semiconductor wafer **, and performing principal component analysis on data to produce first metrics for** wafers

Patent Assignee: LAM RES CORP (LAMR-N)
Inventor: BAILEY A D; MISRA P; YADAV P
Number of Countries: 105 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20040063230	A1	20040401	US 2002414021	P	20020926	200435	B
			US 2002328876	A	20021223		
WO 200430084	A2	20040408	WO 2003US30610	A	20030924	200435	
US 6723574	B1	20040420	US 2002414021	P	20020926	200435	
			US 2002328876	A	20021223		

Priority Applications (No Type Date): US 2002414021 P 20020926; US 2002328876 A 20021223
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20040063230	A1		20	H01L-021/66	Provisional application US 2002414021
WO 200430084	A2	E		H01L-021/66	
US 6723574	B1			G01R-031/26	Provisional application US 2002414021

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NI NO NZ OM PG PH PL PT RO RU SC SD SE SG SK SL SY TJ TM TN TR TT TZ UA UG US UZ VC VN YU ZA ZM ZW
Designated States (Regional): AT BE BG CH CY CZ DE DK EA EE ES FI FR GB GH GM GR HU IE IT KE LS LU MC MW MZ NL OA PT RO SD SE SI SK SL SZ TR TZ UG ZM ZW

Abstract (Basic): US 20040063230 A1

NOVELTY - Determining uniformity metrics of **semiconductor wafer** manufacturing process, comprises: collecting a quantity across each one of first **semiconductor wafers** ; scaling collected quantity data; and performing principal component analysis (PCA) on collected, scaled quantity data to produce first metrics for first **semiconductor wafers** , first metrics including first loads matrix and first scores

matrix.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(a) correlating a nonuniformity to a process variable comprising: collecting a first quantity across each one of first **semiconductor wafers** ; scaling the collected first quantity data; performing a PCA on the collected, scaled first quantity data to produce first metrics for the first **semiconductor wafers** , the first metrics including a first loads matrix and a first scores matrix; identifying a subset of significant loads from the first loads matrix; changing a selected process variable; collecting a second quantity data for second **semiconductor wafers** ; scaling the collected second quantity data for the second **semiconductor wafers** ; projecting the second set of scaled data on the first subset of significant loads to identify projected scores; and correlating the selected process variable with the projected scores; and

(b) a system for quantifying uniformity pattern and determining a correlation between a process variable and a nonuniformity on a **semiconductor wafer** , comprising: a scanning device that has the capability of measuring a quantity at locations of each one of **wafers** ; a **database** that includes process variables and the measured quantities at corresponding locations for each one of the **wafers** , the **database** coupled to the scanning device; a processor coupled to the **database** ; a logic that determines uniformity metrics of a **semiconductor wafer** manufacturing process for first **semiconductor wafers** and second **semiconductor wafers** ; and a logic that correlates a nonuniformity to a process variable.

USE - For determining uniformity metrics of a **semiconductor wafer** manufacturing process (claimed).

ADVANTAGE - The method can objectively and accurately quantify a nonuniformity and correlate the nonuniformity to any relevant change in the system (for e.g. process variable, hardware change).

pp; 20 DwgNo 0/8

Title Terms: DETERMINE; UNIFORM; **SEMICONDUCTOR** ; **WAFER** ; MANUFACTURE; PROCESS; SCALE; COLLECT; QUANTITY; DATA; FIRST; **SEMICONDUCTOR** ; **WAFER** ; PERFORMANCE; PRINCIPAL; COMPONENT; ANALYSE; DATA; PRODUCE; FIRST; **WAFER**

Derwent Class: L03; S02; S03; T01; U11

International Patent Class (Main): G01R-031/26; H01L-021/66

International Patent Class (Additional): G01B-005/28; G01B-005/30; **G06F-019/00**

File Segment: CPI; EPI

10/5/13 (Item 4 from file: 350)

DIALOG(R)File 350:Derwent WPIX

015838558 **Image available**

WPI Acc No: 2003-900762/200382

XRPX Acc No: N03-719141

Manufacturing execution system for semiconductor wafer **fabrication, includes special** database **to** store **set of records having information regarding special operation to be performed on** semiconductor wafer

Patent Assignee: WANGHONG ELECTRONICS CO LTD (WANG-N); LIN C (LINC-I); SU Y (SUYY-I); YU C (YUCC-I)

Inventor: LIN Z; SU Y; YOU Z; LIN C; YU C

Number of Countries: 003 Number of Patents: 003

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030204528	A1	20031030	US 2002136754	A	20020430	200382	B
JP 2003324046	A	20031114	JP 2002206689	A	20020716	200382	
CN 1455436	A	20031112	CN 2003122298	A	20030424	200412	

Priority Applications (No Type Date): US 2002136754 A 20020430

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030204528	A1		10	G06F-007/00	

JP 2003324046 A 9 H01L-021/02
CN 1455436 A H01L-021/00

Abstract (Basic): US 20030204528 A1

NOVELTY - A manufacturing execution system (MES) includes special **database** for **storing** set of records having information regarding special operation to be performed on **semiconductor wafer** , when positioned within process tool.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(1) **semiconductor wafer** fabrication system; and

(2) manufacturing execution method.

USE - For **semiconductor** fabrication system (claimed) used during **integrated circuit** (**IC**) fabrication.

ADVANTAGE - An alarm signal in provided to process tool, if operation data does not match any one of first and second set of records.

DESCRIPTION OF DRAWING(S) - The figure shows **semiconductor wafer** fabrication system including **wafer** fabrication processing tool operably coupled to manufacturing execution system (MES) including basic **database** and special engineer requirement (SER) **database** .

pp; 10 DwgNo 1/4

Title Terms: MANUFACTURE; EXECUTE; SYSTEM; **SEMICONDUCTOR** ; **WAFER** ; FABRICATE; SPECIAL; **DATABASE** ; **STORAGE** ; SET; RECORD; INFORMATION; SPECIAL; OPERATE; PERFORMANCE; **SEMICONDUCTOR** ; **WAFER**

Derwent Class: T01; U11

International Patent Class (Main): **G06F-007/00** ; H01L-021/00; H01L-021/02

International Patent Class (Additional): G05B-019/418; **G06F-017/60**

File Segment: EPI

10/5/15 (Item 6 from file: 350)

DIALOG(R)File 350:Derwent WPIX

015437001 **Image available**

WPI Acc No: 2003-499143/200347

XRPX Acc No: N03-396973

Lot management method for manufacturing semiconductor wafer , **involves changing lot division and lot unification, during process flow, according to data retrieved from** database **based on identification data of** wafer

Patent Assignee: SHARP KK (SHAF)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2003150228	A	20030523	JP 2001346314	A	20011112	200347	B

Priority Applications (No Type Date): JP 2001346314 A 20011112

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2003150228	A		25	G05B-019/418	

Abstract (Basic): JP 2003150228 A

NOVELTY - A host computer (11) accesses a lot status- control **database** (16) to retrieve data describing lot division position and lot unification position, based on identification data of a **wafer** , in response to instructions received through an input/output interface (2). A controller (1) changes lot division and lot unification, during process flow, according to the retrieved data.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(1) lot management apparatus;

(2) lot control program; and

(3) recorded medium **storing** lot control program.

USE - For manufacturing **semiconductor wafer** .

ADVANTAGE - Enables to perform production control of more complicated process flow easily.

DESCRIPTION OF DRAWING(S) - The figure shows the lot **management system** . (Drawing includes non-English language text).
controller (1)
input/output interface (2)
host computer (11)
lot status-control **database** (16)
pp; 25 DwgNo 1/16
Title Terms: LOT; MANAGEMENT; METHOD; MANUFACTURE; **SEMICONDUCTOR** ; **WAFER** ; CHANGE; LOT; DIVIDE; LOT; UNIFIED; PROCESS; FLOW; ACCORD; DATA; RETRIEVAL; **DATABASE** ; BASED; IDENTIFY; DATA; **WAFER**
Derwent Class: T01; T06; U11
International Patent Class (Main): G05B-019/418
International Patent Class (Additional): **G06F-017/60**
File Segment: EPI

10/5/17 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015269124 **Image available**
WPI Acc No: 2003-330053/200331
XRPX Acc No: N03-264162
Pattern data generation system for semiconductor **device manufacture, generates** mask **pattern** data based **on generated master chip layout information and** stored **chip division information**
Patent Assignee: TOSHIBA KK (TOKE); WATANABE S (WATA-I); YANO M (YANO-I)
Inventor: WATANABE S; YANO M
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030009739	A1	20030109	US 2002191591	A	20020708	200331	B
JP 2003022952	A	20030124	JP 2001206541	A	20010706	200331	

Priority Applications (No Type Date): JP 2001206541 A 20010706
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030009739	A1		17	G06F-017/50	
JP 2003022952	A		16	H01L-021/027	

Abstract (Basic): US 20030009739 A1
NOVELTY - A **storage** unit (21) registers chip division information so that pattern data of enlarged **reticle** chip pattern fits into master **mask** pattern region. A chip layout generator generates layout information of master chip by sequentially allotting subpatterns to a master **mask** . A pattern generator generates master **mask** pattern **data based** on the generated master **mask** chip layout and **stored** chip division information.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for the following:
(1) pattern data generation method;
(2) computer program product for controlling pattern data generation;
(3) **reticle** fabrication method; and
(4) **semiconductor** device manufacturing method.
USE - For manufacturing **semiconductor** devices.
ADVANTAGE - Since the pattern data is generated based on the generated master **mask** chip layout and **stored** chip division information, the mistakes occurring during design of pattern is eliminated, thereby the fabrication process of the **semiconductor** device is simplified and the manufacturing cost is reduced.
DESCRIPTION OF DRAWING(S) - The figure shows the functional block diagram of the pattern data generation system.
storage unit (21)
pp; 17 DwgNo 4/8
Title Terms: PATTERN; DATA; GENERATE; SYSTEM; **SEMICONDUCTOR** ; DEVICE; MANUFACTURE; GENERATE; **MASK** ; PATTERN; DATA; BASED; GENERATE; MASTER;

CHIP; LAYOUT; INFORMATION; **STORAGE** ; CHIP; DIVIDE; INFORMATION
Derwent Class: P84; T01; U11
International Patent Class (Main): **G06F-017/50** ; H01L-021/027
International Patent Class (Additional): G03F-001/08; G03F-007/20
File Segment: EPI; EngPI

10/5/18 (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014797836 **Image available**
WPI Acc No: 2002-618542/200266
XRPX Acc No: N02-489705
Reticle management system **e.g. for** mask **for fabrication of** semiconductor **device, has bare** reticle stockers **for** storing reticles , **that are easily removed from and inserted into system**
Patent Assignee: ASYST TECHNOLOGIES INC (ASYS-N); BABBS D A (BABB-I); COSENTINO T (COSE-I); FOSNIGHT W J (FOSN-I); PINNA P (PINN-I); SAMMUT M (SAMM-I); ZEMEN R (ZEME-I)
Inventor: BABBS D A; COSENTINO T; FOSNIGHT W J; PINNA P; SAMMUT M; ZEMEN R
Number of Countries: 100 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020094257	A1	20020718	US 2001760147	A	20010112	200266	B
WO 200295542	A2	20021128	WO 2002US21861	A	20020110	200280	
TW 561520	A	20031111	TW 2002100304	A	20020111	200428	

Priority Applications (No Type Date): US 2001760147 A 20010112
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020094257	A1		16	B65G-001/00	
WO 200295542	A2	E		G06F-000/00	

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZM ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZM ZW

TW 561520	A			H01L-021/027	

Abstract (Basic): US 20020094257 A1
NOVELTY - Bare **reticle stockers** (102) for **storing** several **reticles** , are easily removed from and inserted into the **reticle management system** (100). Bare **reticle** transfer robots (108) transfer **reticles** , received through load ports (106), within the system.
USE - **Reticle management system** e.g. for **mask** for fabrication of **semiconductor** device.
ADVANTAGE - The use of bare **stockers** allows the **storage** capacity and footprint of system to be customized and scaled to the manufactures's needs or modified and redeployed after initial installation and hence time and cost are saved.
DESCRIPTION OF DRAWING(S) - The figure shows a perspective view of modular **reticle management system** .
Reticle management system (100)
Bare **reticle stockers** (102)
Load ports (106)
Bare **reticle** transfer robots (108)
pp; 16 DwgNo 1/12
Title Terms: **RETICLE** ; MANAGEMENT; SYSTEM; **MASK** ; FABRICATE; **SEMICONDUCTOR** ; DEVICE; BARE; **RETICLE** ; **STORAGE** ; **RETICLE** ; EASY; REMOVE; INSERT; SYSTEM
Derwent Class: Q35; U11; X25
International Patent Class (Main): B65G-001/00; **G06F-000/00** ; H01L-021/027
File Segment: EPI; EngPI

10/5/19 (Item 10 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014753278 **Image available**
WPI Acc No: 2002-573982/200261
XRPX Acc No: N02-454869
Semiconductor **device manufacturing process control method involves analyzing environmental data by correlating with metrology data using** wafer **identification** data , based **on which manufacturing process control parameters are modified**
Patent Assignee: TOPRAC A J (TOPR-I); ADVANCED MICRO DEVICES INC (ADMI)
Inventor: TOPRAC A J
Number of Countries: 001 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020069349	A1	20020606	US 2000729412	A	20001204	200261	B
US 6560506	B2	20030506	US 2000729412	A	20001204	200338	

Priority Applications (No Type Date): US 2000729412 A 20001204
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020069349	A1		12	G06F-007/38	
US 6560506	B2			G06F-019/00	

Abstract (Basic): US 20020069349 A1
NOVELTY - The environmental data during manufacture of a **semiconductor** device based on the photolithography process, are analyzed by correlating with metrology data using a **wafer** identification data. The manufacturing process control parameters are modified according to the error data determined from the analysis result.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for the following:
(1) **Semiconductor** manufacturing process control apparatus; and
(2) Computer readable medium **storing semiconductor** device manufacturing process control program.
USE - For controlling manufacturing process of **semiconductor** device in industry.
ADVANTAGE - As the environmental data are analyzed and the processing is controlled during the manufacturing of the **semiconductor** device, the effects due to environmental factors are reduced.
DESCRIPTION OF DRAWING(S) - The figure shows the **semiconductor** manufacturing process control apparatus.
pp; 12 DwgNo 1/5
Title Terms: **SEMICONDUCTOR** ; DEVICE; MANUFACTURE; PROCESS; CONTROL; METHOD ; ENVIRONMENT; DATA; CORRELATE; METROLOGY; DATA; **WAFER** ; IDENTIFY; DATA; BASED; MANUFACTURE; PROCESS; CONTROL; PARAMETER; MODIFIED
Derwent Class: T01; T06; U11
International Patent Class (Main): **G06F-007/38** ; **G06F-019/00**
International Patent Class (Additional): **G06F-009/00** ; **G06F-009/44** ; **G06F-015/00** ; H01L-021/00
File Segment: EPI

10/5/20 (Item 11 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014506956 **Image available**
WPI Acc No: 2002-327659/200236
XRPX Acc No: N02-256944
Wafer **management method in automated material handling system, involves accommodating test** wafers **classified into several classes, in cassettes based on production time profile of each class of** wafer
Patent Assignee: ADVANCED MICRO DEVICES INC (ADMI)

Inventor: CONBOY M R; COSS E; RYAN P J
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6338005	B1	20020108	US 99387613	A	19990831	200236	B

Priority Applications (No Type Date): US 99387613 A 19990831
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6338005	B1		11	G06F-007/00	

Abstract (Basic): US 6338005 B1

NOVELTY - The test **wafers** are classified into many classes and a production time profile is determined for each class of **wafer** . The **wafers** are placed into cassettes, based on the determined profile. A request to pick up a particular group of test **wafer** class, is received. A cassette containing the smallest number of groups similar to the particular group of **wafer** class, for which the request is received, is identified.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for **wafer management system** with **stored** software.

USE - For managing **wafers** in automated material handling system, for fabricating **integrated circuits** on **semiconductor wafer** .

ADVANTAGE - Reduces the number of the test cassettes required for determined number of test **wafers** and minimizes duplication of same group of **wafer** in same cassette, and thus increases throughput of **wafer** through the automated material handling system.

DESCRIPTION OF DRAWING(S) - The figure shows the flow diagram explaining the **wafer** management method.

pp; 11 DwgNo 3/5

Title Terms: **WAFER** ; MANAGEMENT; METHOD; AUTOMATIC; MATERIAL; HANDLE; SYSTEM; ACCOMMODATE; TEST; **WAFER** ; CLASSIFY; CLASS; CASSETTE; BASED; PRODUCE; TIME; PROFILE; CLASS; **WAFER**
Derwent Class: T01; U11
International Patent Class (Main): **G06F-007/00**
File Segment: EPI

10/5/21 (Item 12 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014419547 **Image available**
WPI Acc No: 2002-240250/200229
XRPX Acc No: N02-185414

Reticle management system **that provides data** storage **and retrieval of data associated with each** reticle **and of movement and** storage **of** reticles **and their carriers**

Patent Assignee: PRI AUTOMATION INC (PRIA-N); MARIANO T (MARI-I); WIESLER O (WIES-I)
Inventor: MARIANO T; WIESLER O
Number of Countries: 095 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200182055	A1	20011101	WO 2001US13349	A	20010425	200229	B
US 20010047222	A1	20011129	US 2000199453	P	20000425	200229	
			US 2001842370	A	20010425		
AU 200159151	A	20011107	AU 200159151	A	20010425	200229	

Priority Applications (No Type Date): US 2000199453 P 20000425; US 2001842370 A 20010425
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200182055	A1	E	39	G06F-007/00	

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL

PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZW
US 20010047222 A1 G06F-017/00 Provisional application US 2000199453

AU 200159151 A G06F-007/00 Based on patent WO 200182055

Abstract (Basic): WO 200182055 A1

NOVELTY - Bays (101-107) each has a **stocker** (102,104,106,108) that contains lithographic **reticles** or **semiconductor wafers** and one or more processing stations (120-126,128-134,136-142,144-150) for processing the **wafers** . The bays are linked by a transport system (110) for the automatic transport of the **wafers** between the bays with the transport system and the processing stations.

DETAILED DESCRIPTION - AN INDEPENDENT CLAIM is included for a **data managing** apparatus.

USE - Management of **reticles** .

ADVANTAGE - Allowing user to access current data corresponding to various **reticles** .

DESCRIPTION OF DRAWING(S) - The drawing shows a **wafer** processing facility

Bays (101,103,105,107)

Stockers (102,104,106,108)

Processing stations (120-150)

Transport system (110)

pp; 39 DwgNo 1/6

Title Terms: **RETICLE** ; MANAGEMENT; SYSTEM; DATA; **STORAGE** ; RETRIEVAL; DATA; ASSOCIATE; **RETICLE** ; MOVEMENT; **STORAGE** ; **RETICLE** ; CARRY
Derwent Class: T01; U11
International Patent Class (Main): **G06F-007/00** ; **G06F-017/00**
File Segment: EPI

10/5/22 (Item 13 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014393622 **Image available**
WPI Acc No: 2002-214325/200227
XRPX Acc No: N02-163955

Silicon wafer **inspection system in** semiconductor **fabrication line, detects amount of deviations of x-y coordinates of inspected part on preliminary apparatus from x-y coordinates on review apparatus**

Patent Assignee: JOEL LTD (JOEL-N)
Inventor: INOKUCHI M
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6259960	B1	20010710	US 97962585	A	19971031	200227	B

Priority Applications (No Type Date): US 97962585 A 19971031
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6259960	B1		119	G06F-019/00	

Abstract (Basic): US 6259960 B1

NOVELTY - A misalignment correcting unit has detector which detects amount of deviations of x-y coordinates of Si **wafer** position reference point on preliminary inspection apparatus from x-y coordinates of reference point on review apparatus when inspected part is set on inspected part holder. Inspected part is moved to distance equal to detected deviation amount to bring both x-y coordinates into agreement.

DETAILED DESCRIPTION - A computer implemented defect image filing system (3) has a memory **storing** information of part to be inspected e.g. Si **wafer** in **database** which includes a preliminary inspection information **database** and review information **database** . Preliminary

inspection information having part search information which is helpful in identifying defects on already preliminary inspected part and positional information about position of defects present on inspected part determined on a preliminary inspection apparatus, are **stored** in preliminary inspection information **database** . Part search information useful in identifying inspected part and review information obtained by review inspection of preliminary inspected part are **stored** in review information **database** . A review apparatus comprises a microscope and vacuum inspection chamber in which inspected part holder is arranged. An x-y table is provided for moving the inspected part holder in x-y directions perpendicular to each other to bring desired part of inspected part into review position. A microscope image pickup device takes microscope image at a setup magnification. Entered information about search for inspected part set on inspected part holder is **stored** in part search information **storage** . A preliminary information reader reads preliminary inspection information of inspected part from inspected part **database** according to part search information. A defect to be reviewed is selected from defects contained in preliminary inspection information. Review information obtained by reviewing selected defect is **stored** in review information registration unit. An inspected part moving unit moves x-y table to bring inspected part held by holder into target x-y coordinates. A misalignment correcting unit has reference point coinciding movement unit to make inspected part to move distance equal to detected amount of deviations to bring x-y coordinates of inspected part on preliminary inspection apparatus into agreement with x-y coordinates of inspected part on review apparatus.

USE - For detecting presence or absence of defect e.g. adhering foreign matter or defective pattern on silicon **wafer** in **semiconductor** fabrication line.

ADVANTAGE - Preliminary inspection about inspected part is automatically read from inspection part information **database** . Defects that need to be reviewed are automatically selected from preliminary inspection information. Hence amount of operation that operator performs on part inspecting system is reduced and efficiency of work is enhanced. Rotation of **wafer** is corrected by misalignment correcting unit by detecting orientation flat state or notches.

DESCRIPTION OF DRAWING(S) - The figure shows the diagram of part inspecting system.

Image filing system (3)

pp; 119 DwgNo 1/76

Title Terms: SILICON; **WAFER** ; INSPECT; SYSTEM; **SEMICONDUCTOR** ; FABRICATE; LINE; DETECT; AMOUNT; DEVIATE; COORDINATE; INSPECT; PART; PRELIMINARY; APPARATUS; COORDINATE; REVIEW; APPARATUS

Derwent Class: S02; S03; T01; T02; U11

International Patent Class (Main): **G06F-019/00**

International Patent Class (Additional): G06G-007/66

File Segment: EPI

10/5/26 (Item 17 from file: 350)

DIALOG(R)File 350:Derwent WPIX

013972584 **Image available**

WPI Acc No: 2001-456797/200149

XRPX Acc No: N01-338524

Reference wafer **supervising method for** semiconductor **device, involves accommodating reference** wafers **on** storage **shelf collectively without classification according to processing condition in** wafer **processing device**

Patent Assignee: NEC CORP (NIDE); NEC ELECTRONICS CORP (NIDE); NIPPON ELECTRIC CO (NIDE)

Inventor: SUGIKAWA Y

Number of Countries: 005 Number of Patents: 007

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20010007085	A1	20010705	US 2000746343	A	20001222	200149	B

JP 2001185465	A	20010706	JP 99367493	A	19991224	200154
KR 2001062659	A	20010707	KR 200081104	A	20001223	200175
GB 2364437	A	20020123	GB 200031590	A	20001222	200215
GB 2382463	A	20030528	GB 200031590	A	20001222	200335
			GB 200222654	A	20020930	
KR 371291	B	20030207	KR 200081104	A	20001223	200341
TW 512477	A	20021201	TW 2000127802	A	20001222	200353

Priority Applications (No Type Date): JP 99367493 A 19991224
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20010007085	A1		32	G06F-019/00	
JP 2001185465	A		19	H01L-021/02	
KR 2001062659	A			H01L-021/68	
GB 2364437	A			G06F-019/00	
GB 2382463	A			G06F-019/00	Div ex application GB 200031590
KR 371291	B			H01L-021/68	Previous Publ. patent KR 2001062659
TW 512477	A			H01L-021/68	

Abstract (Basic): US 20010007085 A1

NOVELTY - A control system (10) supervises production line with a function of changing the item name of reference **wafer** . A preset common representative name is introduced for several reference **wafers** for evaluation of **wafer** process device (30) and correspondingly reference **wafers** are **stored** on **storage** shelf (20) collectively without classification according to processing conditions in **wafer** process device.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(a) **Storage** shelf for **storing** reference **wafer** ;

(b) Production control system for supervising **wafer** ;

(c) Reference **wafer** supervising system;

(d) Reference **wafer management system**

USE - Used in production line of **semiconductor** devices for supervising reference **wafer** used for testing, evaluation, maintenance and inspection of **wafer** .

ADVANTAGE - Enables processing of product lot to be halted immediately when the measured result of reference **wafer** is negative. Since several reference **wafers** are **stored** on the shelf collectively without classifying the **wafers** according to processing conditions, the number of reference **wafers** **stored** on the shelf is reduced. Thus shelf space for accommodating the reference **wafers** is utilized efficiently.

DESCRIPTION OF DRAWING(S) - The figure shows the configuration for **wafer** supervising.

Control system (10)

Storage shelf (20)

Water process device (30)

pp; 32 DwgNo 1/17

Title Terms: REFERENCE; **WAFER** ; SUPERVISION; METHOD; **SEMICONDUCTOR** ; DEVICE; ACCOMMODATE; REFERENCE; **WAFER** ; **STORAGE** ; SHELF; COLLECT; CLASSIFY; ACCORD; PROCESS; CONDITION; **WAFER** ; PROCESS; DEVICE
Derwent Class: T01; T06; U11
International Patent Class (Main): **G06F-019/00** ; H01L-021/02; H01L-021/68
International Patent Class (Additional): C23C-016/44; G05B-015/02; **G06F-017/60** ; H01L-021/00
File Segment: EPI

10/5/28 (Item 19 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013960592 **Image available**
WPI Acc No: 2001-444806/200148
XRPX Acc No: N01-328797
Inspection data processing procedure for defect inspection of

semiconductor wafer , **involves producing recognition** data based **on threshold defects level corresponding to each defect existence area**
Patent Assignee: HITACHI LTD (HITA)
Inventor: MAEDA S; OKA K; SHIBA M; SHIMODA A; YOSHITAKE Y
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2000306964	A	20001102	JP 99115296	A	19990422	200148	B
US 6456951	B1	20020924	US 99225513	A	19990106	200266	
			US 2000553944	A	20000421		

Priority Applications (No Type Date): JP 99115296 A 19990422
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2000306964	A		19	H01L-021/66	
US 6456951	B1			G06F-011/32	CIP of application US 99225513

Abstract (Basic): JP 2000306964 A
NOVELTY - The coordinate data and characteristics data corresponding to detected defect in each **wafer** area is acquired. Based on threshold defect level, recognition data corresponding to detected defects existence area is produced. The information indicating defect level of defect is **stored** in the **database** (24), based on the recognition data.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for inspection data processor.
USE - For processing inspection data of **semiconductor wafer** , during foreign material inspection, short-circuit inspection, discontinuity inspection during manufacture of **semiconductor** device.
ADVANTAGE - Since level of defect is acquired for each defect area, efficient review and analysis of defect is performed.
DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of inspection data processor.
Database (24)
pp; 19 DwgNo 1/20
Title Terms: INSPECT; DATA; PROCESS; PROCEDURE; DEFECT; INSPECT; **SEMICONDUCTOR** ; **WAFER** ; PRODUCE; RECOGNISE; DATA; BASED; THRESHOLD; DEFECT; LEVEL; CORRESPOND; DEFECT; EXIST; AREA
Derwent Class: S01; S03; T01; U11
International Patent Class (Main): **G06F-011/32** ; H01L-021/66
International Patent Class (Additional): G01N-021/88; G01R-031/02
File Segment: EPI

10/5/29 (Item 20 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013107069 **Image available**
WPI Acc No: 2000-278940/200024
XRPX Acc No: N00-210283
Automated semiconductor **manufacturing processing** management system **in** semiconductor wafer **process factory, has server which searches** database **to output manufacturing data depending on request from user terminal**
Patent Assignee: OKI ELECTRIC IND CO LTD (OKID)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2000077290	A	20000314	JP 98244102	A	1998082	200024	B

Priority Applications (No Type Date): JP 98244102 A 19980828
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2000077290	A		19	H01L-021/02	

Abstract (Basic): JP 2000077290 A
NOVELTY - Photograph image data of **semiconductor wafer** surface,

input **wafer** processing data and table showing relation between image data and image are **stored** in **database** (2). When inquiry of process data is received by server (1) from terminal (6), **database** is searched and corresponding process data is sent to terminal.

USE - For management of automated **semiconductor wafer** manufacturing process in factory, etc.

ADVANTAGE - As operator is enabled to comment using image data for **wafer** inspection and process log information, inspection information is increased.

DESCRIPTION OF DRAWING(S) - The figure shows schematic control diagram of automatic **semiconductor wafer** production system.

Server (1)

Database (2)

Terminal (6)

pp; 19 DwgNo 1/20

Title Terms: AUTOMATIC; **SEMICONDUCTOR** ; MANUFACTURE; PROCESS; MANAGEMENT; SYSTEM; **SEMICONDUCTOR** ; **WAFER** ; PROCESS; FACTORY; SERVE; SEARCH; **DATABASE** ; OUTPUT; MANUFACTURE; DATA; DEPEND; REQUEST; USER; TERMINAL

Derwent Class: T01; U11

International Patent Class (Main): H01L-021/02

International Patent Class (Additional): **G06F-017/60** ; H01L-021/66

File Segment: EPI

10/5/30 (Item 21 from file: 350)

DIALOG(R)File 350:Derwent WPIX

012674523 **Image available**

WPI Acc No: 1999-480630/199941

XRPX Acc No: N99-357963

Real-time in-situ interactive supervision of a determined step for fabricating a semiconductor wafer

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC); SOFIE INSTR (SOFI-N); IBM CORP (IBMC)

Inventor: CANTELOUP J; CORONEL P; MACCAGNAN R; VASSILAKIS J

Number of Countries: 026 Number of Patents: 004

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 932194	A1	19990728	EP 97480104	A	19971230	199941	B
JP 2000003842	A	20000107	JP 98338911	A	19981130	200012	
JP 3024759	B2	20000321	JP 98338911	A	19981130	200019	
US 6363294	B1	20020326	US 98222498	A	19981229	200226	

Priority Applications (No Type Date): EP 97480104 A 19971230

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 932194	A1	E	30	H01L-021/66	
	Designated States (Regional): AL AT BE CH DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI				
JP 2000003842	A		21	H01L-021/02	
JP 3024759	B2		21	H01L-021/02	Previous Publ. patent JP 2000003842
US 6363294	B1			G06F-019/00	

Abstract (Basic): EP 932194 A1

NOVELTY - Selects at least one process parameter and establishes a **database** for it which includes alarm conditions and **wafer** history.

DETAILED DESCRIPTION - The method for real-time in-situ interactive supervision of a determined step of a process for fabricating a **semiconductor wafer** belonging to a batch of **wafers** comprising the preliminary steps of:

(a) selecting at least one process parameter that is determining for the monitoring of that determined step;

(b) establishing a **database** including:

(i) a first file referred to as the alarm component of this **database** which contains in coded form:

(1) the evolution of the selected process parameter in normal

operating conditions and in all the deviations thereof identified by process engineers;

(2) algorithms representative of the analysis rules defined by process engineers adapted to recognize any such deviation which include rejection criteria for each deviation; and

(3) an alert code for each case of deviation;

(ii) a second file referred to as the **wafer** history component of this **database** which contains in coded form the history of the **wafer** until this step with a reference to the batch, the process and the step names for that determined step and the identification number of the **wafer** in consideration; wherein the **wafer** history includes the important process parameters and the evolution of the selected process parameter for the previous process steps still for the **wafer** in consideration; the method further comprising for that determined step, the steps of:

(c) providing:

(i) a tool having at least one chamber for processing the **wafer** at the determined step of the fabrication process;

(ii) a tool computer to control the physical process parameters of the tool;

(iii) at least one monitoring equipment, to monitor at least one selected process parameter that is determining for the step;

(iv) at least one measurement unit internally mounted in the monitoring equipment and/or in the process tool that is capable to perform in-situ process parameter measurements;

(v) a supervisor that is connected through a network to the computer, the monitoring equipment, the measurement unit and the **database** to supervise the process flow for the determined step;

(d) introducing the **wafer** in the tool chamber;

(e) in-situ measuring a determined process parameter (e.g. a thickness) with the measurement unit, the value of which is **stored** in the **database** for immediate or subsequent use;

(f) retrieving the value from the **database** for immediate exploitation in the determined step to update at least one process parameter (e.g. an etch rate) to change the operating conditions thereof;

(g) starting **wafer** processing

(h) permanently analyzing the evolution of the selected process parameter by the supervisor for comparison with the corresponding data **stored** in the **database** to detect in real-time in-situ any deviation that could occur during the determined step;

(i) continuing **wafer** processing to normal end if no deviation is detected and in the contrary taking the corrective action defined by the alert code corresponding to the detected deviation.' and,

(j) **storing** all the data that are representative of the processing for the determined step in a so-called step report and the alert code (if any) in an alarm report to update the **wafer** history file of the **wafer** in consideration.

USE - The method is used for supervision of e.g. etching, deposition etc.

ADVANTAGE - Reacts in real-time to problems during the current processing step.

DESCRIPTION OF DRAWING(S) - The drawing shows the processing system with the supervision system added to it.

pp; 30 DwgNo 7/18

Title Terms: REAL; TIME; SITU; INTERACT; SUPERVISION; DETERMINE; STEP; FABRICATE; **SEMICONDUCTOR** ; **WAFER**

Derwent Class: T01; T06; U11; V05; X12

International Patent Class (Main): **G06F-019/00** ; H01L-021/02; H01L-021/66

International Patent Class (Additional): H01L-021/3065

File Segment: EPI

10/5/31 (Item 22 from file: 350)

011886555 **Image available**
WPI Acc No: 1998-303465/199827
XRPX Acc No: N98-238040
Process management system **in** semiconductor wafer **factory** - stores **information related to existing** wafer **to be processed in lot information** database
Patent Assignee: SONY CORP (SONY)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 10106906	A	19980424	JP 96262065	A	19961002	199827	B

Priority Applications (No Type Date): JP 96262065 A 19961002
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 10106906	A		11	H01L-021/02	

Abstract (Basic): JP 10106906 A
The system manages the **semiconductor wafer** which is to be inserted into a processing apparatus per lot. The information related to the existing **wafer** is **stored** in a lot information **database** (10a). The production command of the lot which uses the existing **wafer** is received. The information **stored** in the **database** is displayed on the screen of the display device.
The selection of the existing **wafer** is received by an input device. The organisation of the novel lot is done with the selected existing **wafer** . A lot registration unit (10b) **stores** the information on the novel lot in the lot information **database** .
ADVANTAGE - Prevents missing of input. Enables to check suitability of lot insertion. Eliminates insertion of mistaken lot.
Dwg.1/9
Title Terms: PROCESS; MANAGEMENT; SYSTEM; **SEMICONDUCTOR** ; **WAFER** ; FACTORY ; **STORAGE** ; INFORMATION; RELATED; EXIST; **WAFER** ; PROCESS; LOT; INFORMATION; **DATABASE**
Derwent Class: T01; U11
International Patent Class (Main): H01L-021/02
International Patent Class (Additional): **G06F-017/60**
File Segment: EPI

10/5/32 (Item 23 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011799850 **Image available**
WPI Acc No: 1998-216760/199819
XRPX Acc No: N98-171382
Downsizing graphic data of mask **pattern in hierarchical graphic** database **in fabrication of** integrated circuits **- downsizing, flattening and oversizing** database **to form integral graphic element of individual abutting elements, undersizing** database , **and performing logical-NOT operation on undersized** database **and flattened** database
Patent Assignee: WINBOND ELECTRONICS CORP (WINB-N)
Inventor: YANG S
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5731986	A	19980324	US 96643359	A	19960506	199819	B

Priority Applications (No Type Date): US 96643359 A 19960506
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5731986	A		24	G06F-017/50	

Abstract (Basic): US 5731986 A
The method includes the steps of:
(1) downsizing the hierarchical graphic **database** ;

(2) flattening the downsized hierarchical graphic **database** ;
(3) oversizing the flattened hierarchical graphic **database** ;
(4) undersizing the oversized hierarchical graphic **database** ;
(5) performing a logical-NOT operation on the undersized hierarchical graphic **database** and the flattened hierarchical graphic **database** so as to obtain a gap-filling graphic element; and
(6) incorporating the gap-filling graphic element in the downsized hierarchical graphic **database** .

USE - Downsizing graphic data of **mask** pattern **stored** in hierarchical graphic **database** so that **mask** pattern can be used in fabrication of **integrated circuits** having reduced feature size.

ADVANTAGE - Filling gaps formed between abutting graphic elements with supplementary graphic elements, without disturbing or modifying overall hierarchical structure for recording and relating all graphic elements in **mask** pattern. Downsizes graphic data of **mask** pattern without increasing amount of required data **storage** in hierarchical graphic **database** , which would burden **storage** , transmission, and modification capacities of **mask** pattern.

Dwg.5/6

Title Terms: GRAPHIC; DATA; **MASK** ; PATTERN; HIERARCHY; GRAPHIC; **DATABASE** ; FABRICATE; INTEGRATE; CIRCUIT; FLATTEN; **DATABASE** ; FORM; INTEGRAL; GRAPHIC; ELEMENT; INDIVIDUAL; ABUT; ELEMENT; **DATABASE** ; PERFORMANCE; LOGIC; OPERATE; UNDERSIZE; **DATABASE** ; FLATTEN; **DATABASE**
Derwent Class: T01
International Patent Class (Main): **G06F-017/50**
File Segment: EPI

10/5/34 (Item 25 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011484506 **Image available**
WPI Acc No: 1997-462411/199743
XRPX Acc No: N97-385120

Mask **pattern designing appts for producing** photomask **used in mfr of high density** IC **e.g. LSI, VLSI - has optical intensity distribution simulator which computes optical intensity distribution of water based on edited graphic data and** stores **it in** storage **unit as file**

Patent Assignee: DAINIPPON PRINTING CO LTD (NIPQ)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 9212543	A	19970815	JP 9639127	A	19960202	199743	B

Priority Applications (No Type Date): JP 9639127 A 19960202
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 9212543	A		7	G06F-017/50	

Abstract (Basic): JP 9212543 A

The appts includes a **mask** pattern designing unit (120) which forms graphic **data based** on predetermined instructions input from an input unit (110). A **mask** pattern data in the form of graphic data is **stored** in a **mask** pattern **data file storage** unit (122). The graphic data is displayed on a **mask** pattern display unit (160).

An optical intensity distribution simulator (130) computes the optical intensity distribution of **wafer** corresponding to edited graphic data from a graphic edit unit (140). The simulator outputs a simulation data which comprises an ensemble of computed optical intensity distribution simulation data. The simulation data is **stored** in an optical intensity distribution simulation file **storage** unit (132) as a file.

ADVANTAGE - Shortens **mask** data production time.

Dwg.1/4

Title Terms: **MASK** ; PATTERN; DESIGN; APPARATUS; PRODUCE; **PHOTOMASK** ; MANUFACTURE; HIGH; DENSITY; **IC** ; LSI; VLSI; OPTICAL; INTENSITY;

DISTRIBUTE; SIMULATE; COMPUTATION; OPTICAL; INTENSITY; DISTRIBUTE; WATER; BASED; EDIT; GRAPHIC; DATA; **STORAGE** ; **STORAGE** ; UNIT; FILE
Derwent Class: T01; U11
International Patent Class (Main): **G06F-017/50**
International Patent Class (Additional): H01L-021/82
File Segment: EPI

10/5/37 (Item 28 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008618646 **Image available**
WPI Acc No: 1991-122676/199117
XRPX Acc No: N91-094214
Data storage **system for** semiconductor **-device production - creates** data - base **in which** wafer **numbers grouped under production process conditions are registered NoAbstract Dwg 1/7**
Patent Assignee: MATSUSHITA ELEC IND CO LTD (MATU)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 3063736	A	19910319	JP 89198971	A	19890731	199117	B

Priority Applications (No Type Date): JP 89198971 A 19890731
Title Terms: DATA; **STORAGE** ; SYSTEM; **SEMICONDUCTOR** ; DEVICE; PRODUCE; DATA; BASE; **WAFER** ; NUMBER; GROUP; PRODUCE; PROCESS; CONDITION; REGISTER ; NOABSTRACT
Derwent Class: T01; U11
International Patent Class (Additional): **G06F-012/00** ; H01L-021/66
File Segment: EPI
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t s11/5/1-4

11/5/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

016181990 **Image available**
WPI Acc No: 2004-339877/200431
XRPX Acc No: N04-271751
Automated semiconductor wafer **handling system comprises computer integrated manufacturing system in operative communication with real-time dispatch system for automating equipment within** wafer **fabrication system**
Patent Assignee: TAIWAN SEMICONDUCTOR MFG CO LTD (TASE-N)
Inventor: CHANG K; CHUE J; LIU J; SHIH J; WANG M
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20040073331	A1	20040415	US 2002268379	A	20021010	200431	B

Priority Applications (No Type Date): US 2002268379 A 20021010
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20040073331	A1		10	G06F-007/00	

Abstract (Basic): US 20040073331 A1
NOVELTY - A **stocker** (20) embeds a sorter (22) for sorting **wafers** within front opening unified pods (FOUPs) which are in operative communication with a computer integrated manufacturing (CIM) system (28). A CIM system in operative communication with real-time dispatch system (16), controlling dispatching of **wafer** lot orders within **wafer** fabrication system automates equipment within the fabrication system.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for automated material handling system usage method.
USE - For **wafer** processing within automated **wafer** fabrication system.
ADVANTAGE - Prevents bottlenecks from occurring during sorting of **wafers** . Also reduces a bottleneck in intrabay or interbay transportation. Automates splitting, merging, FOUP exchanges, FOUP cleanings and **wafer** map verifications to improve production throughput while reducing mis-operation. Improves equipment's utilization and production throughput.
DESCRIPTION OF DRAWING(S) - The figure shows an overview of automated **semiconductor wafer** handling system.
front opening unified pod **management system** (12)
real-time dispatch system (16)
integration system (18)
stocker (20)
sorter (22)
CIM system (28)
pp; 10 DwgNo 1/3
Title Terms: AUTOMATIC; **SEMICONDUCTOR** ; **WAFER** ; HANDLE; SYSTEM; COMPRISE; COMPUTER; INTEGRATE; MANUFACTURE; SYSTEM; OPERATE; COMMUNICATE; REAL; TIME; DISPATCH; SYSTEM; AUTOMATIC; EQUIPMENT; **WAFER** ; FABRICATE; SYSTEM
Derwent Class: T01; U11
International Patent Class (Main): **G06F-007/00**
File Segment: EPI

11/5/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

016066735 **Image available**
WPI Acc No: 2004-224586/200421
XRPX Acc No: N04-177389

Foreign matter monitoring system for semiconductor **manufacturing, has image signal processing unit to check matter based on inspection recipes selected for matter based on control information and detected digital image signal**

Patent Assignee: HITACHI DENSHI ENG KK (HISB); HITACHI LTD (HITA); NISHIYAMA H (NISH-I); NOGUCHI M (NOGU-I); SEKIGUCHI T (SEKI-I); WATANABE T (WATA-I)

Inventor: NISHIYAMA H; NOGUCHI M; SEKIGUCHI T; WATANABE T

Number of Countries: 002 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20040021856	A1	20040205	US 2003630734	A	20030731	200421	B
JP 2004071671	A	20040304	JP 2002225692	A	20020802	200421	

Priority Applications (No Type Date): JP 2002225692 A 20020802

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20040021856	A1		48	G01N-021/88	
JP 2004071671	A		30	H01L-021/02	

Abstract (Basic): US 20040021856 A1

NOVELTY - The system has a base system with a control unit to acquire control information and a buffer memory to **store** a detection digital image signal (124) obtained from each foreign matter monitor. A **database stores** inspection recipes each related to one monitor. An image signal processing unit checks matter based on the recipes selected for corresponding matter based on control information and detected digital image signal.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following :

(1) a process processing apparatus

(2) a method of electronic commerce.

USE - Used for monitoring foreign matter during **semiconductor** manufacturing.

ADVANTAGE - The system finds dust in any process of a **semiconductor** device as early as possible such that the influence of the process dusting is limited to a minimum number of **wafers** , thereby eliminating mass failures.

DESCRIPTION OF DRAWING(S) - The drawing shows a front view of a compact foreign matter monitor set up in each process operation machine.

Illumination light source (111)

Condenser lens (113)

Focusing lens (122)

Digital image signal (124)

Control device (135)

pp; 48 DwgNo 4/40

Title Terms: FOREIGN; MATTER; MONITOR; SYSTEM; **SEMICONDUCTOR** ; MANUFACTURE ; IMAGE; SIGNAL; PROCESS; UNIT; CHECK; MATTER; BASED; INSPECT; RECIPE; SELECT; MATTER; BASED; CONTROL; INFORMATION; DETECT; DIGITAL; IMAGE; SIGNAL

Derwent Class: S01; S03; T01; T05; U11

International Patent Class (Main): G01N-021/88; H01L-021/02

International Patent Class (Additional): G05B-019/418; **G06F-017/60** ; G06T-001/00; H01L-021/66

File Segment: EPI

11/5/3 (Item 3 from file: 350)

DIALOG(R)File 350:Derwent WPIX

016044280 **Image available**

WPI Acc No: 2004-202131/200419

XRPX Acc No: N04-160668

Automatic bill-of-material production system for semiconductor **product, automatically prepares bill-of-materials using prepared graphical data**

for block of mask **component number, to satisfy customer deliverable order**
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Inventor: BALLAS D F; BICKFORD J P S; MAHEUX T R; MCLAUGHLIN P G; POULIN D L
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20040019538	A1	20040129	US 200264539	A	20020725	200419	B

Priority Applications (No Type Date): US 200264539 A 20020725
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20040019538	A1		18	G06F-017/60	

Abstract (Basic): US 20040019538 A1
NOVELTY - A relational **database** tool (108) automatically prepares the bill-of-materials (BOM) using prepared graphical data for block of **mask** component numbers, to satisfy the customer deliverable order for a **semiconductor** product. The graphical data is provided by a data preparation tool.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:
(1) method of automatically producing BOM for **semiconductor mask** ; and
(2) BOM preparation program **storage** device.
USE - For producing bill-of-material (BOM) of **semiconductor** product such as **semiconductor** chip.
ADVANTAGE - The system provides capability to plan the capacity for manufacturing sub-components before the components are developed. Predicts the cost of the **mask** , cost of the product and altering the aspects of the product with changes to the **mask** design.
DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of the automatic bill-of-material production system.
ordering system (102)
product manager tool (104)
relational **database** tool (108)
manufacturing panning engine (110)
forecast tool (114)
pp; 18 DwgNo 1/7
Title Terms: AUTOMATIC; BILL; MATERIAL; PRODUCE; SYSTEM; **SEMICONDUCTOR** ; PRODUCT; AUTOMATIC; PREPARATION; BILL; MATERIAL; PREPARATION; GRAPHICAL; DATA; BLOCK; **MASK** ; COMPONENT; NUMBER; SATISFY; CUSTOMER; DELIVER; ORDER
Derwent Class: T01; U11
International Patent Class (Main): **G06F-017/60**
File Segment: EPI

11/5/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014419547 **Image available**
WPI Acc No: 2002-240250/200229
XRPX Acc No: N02-185414
Reticle management system **that provides data** storage **and retrieval of data associated with each** reticle **and of movement and** storage **of** reticles **and their carriers**
Patent Assignee: PRI AUTOMATION INC (PRIA-N); MARIANO T (MARI-I); WIESLER O (WIES-I)
Inventor: MARIANO T; WIESLER O
Number of Countries: 095 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200182055	A1	20011101	WO 2001US13349	A	20010425	200229	B
US 20010047222	A1	20011129	US 2000199453	P	20000425	200229	
			US 2001842370	A	20010425		

AU 200159151 A 20011107 AU 200159151 A 20010425 200229

Priority Applications (No Type Date): US 2000199453 P 20000425; US 2001842370 A 20010425

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200182055	A1	E	39	G06F-007/00	

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW

Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZW

US 20010047222 A1 G06F-017/00 Provisional application US 2000199453

AU 200159151 A G06F-007/00 Based on patent WO 200182055

Abstract (Basic): WO 200182055 A1

NOVELTY - Bays (101-107) each has a **stocker** (102,104,106,108) that contains lithographic **reticles** or **semiconductor wafers** and one or more processing stations (120-126,128-134,136-142,144-150) for processing the **wafers** . The bays are linked by a transport system (110) for the automatic transport of the **wafers** between the bays with the transport system and the processing stations.

DETAILED DESCRIPTION - AN INDEPENDENT CLAIM is included for a **data managing** apparatus.

USE - Management of **reticles** .

ADVANTAGE - Allowing user to access current data corresponding to various **reticles** .

DESCRIPTION OF DRAWING(S) - The drawing shows a **wafer** processing facility

Bays (101,103,105,107)

Stockers (102,104,106,108)

Processing stations (120-150)

Transport system (110)

pp; 39 DwgNo 1/6

Title Terms: **RETICLE** ; MANAGEMENT; SYSTEM; DATA; **STORAGE** ; RETRIEVAL; DATA; ASSOCIATE; **RETICLE** ; MOVEMENT; **STORAGE** ; **RETICLE** ; CARRY

Derwent Class: T01; U11

International Patent Class (Main): **G06F-007/00** ; **G06F-017/00**

File Segment: EPI

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Set	Items	Description
S1	151705	RETICLE? OR MASK? OR PHOTOMASK? OR WAFER? OR RETICULE?
S2	736825	STOCKER? OR STORAGE? OR INVENTORY? OR INVENTORI? OR WAREHOUS? OR SUPPLY? OR SUPPLIE???
S3	272019	SEMICONDUCTOR? OR INTEGRATED()CIRCUIT? OR IC OR ICS
S4	197673	DATABASE? OR DATA()BASE? OR DB OR DBS OR DBMS OR MANAGEMENT()SYSTEM? OR DATABANK? OR DATA()BANK? OR DATAFILE? OR DATA()FILE? OR DATA()MANAG?
S5	441	S1(3N)S4
S6	11644	S2(3N)S4
S7	13	S5(S)S6 AND S3
S8	616	S1(5N)S4
S9	16003	S2(5N)S4
S10	86	S8 AND S9 AND S3
S11	46	S10 AND CENTRAL?
S12	28	S11 AND CONTROLLER?
S13	21	S12 NOT S7

?show files
File 348:EUROPEAN PATENTS 1978-2004/Jun W01
(c) 2004 European Patent Office
File 349:PCT FULLTEXT 1979-2002/UB=20040603,UT=20040527
(c) 2004 WIPO/Univentio
?

?t s7/3,k/6,9,11,12

7/3,K/6 (Item 3 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00961430 **Image available**
WORKPIECE SORTER OPERATING WITH MODULAR BARE WORKPIECE STOCKERS AND/OR CLOSED CONTAINER STOCKERS
TRIEUSE DE PIECES A USINER FONCTIONNANT AVEC DES STOCKEURS DE PIECES A USINER OUVERTS MODULAIRES ET/OU DES STOCKEURS A RECIPIENTS FERMES

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Application: WO 2002US21861 20020110 (PCT/WO US0221861)
Priority Application: US 2001760147 20010112
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(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZM ZW
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Fulltext Availability:
Detailed Description
Claims

English Abstract
A **reticle management system** is disclosed including a sorter (101) coupled to one or more stockers (102) that allow a customized configuration of the overall **reticle management system** . The **stockers** may be bare reticle stockers, closed container reticle stockers, or both. In embodiments of the present invention, the **reticle management system** includes between one and six individual bare reticle stockers and/or closed container stockers for...

Detailed Description
... plurality of modular bare reticle stockers and/or closed container stockers.

DescLiption of Related Art
Semiconductor devices on wafers are made up of as many as fifty individual patterned layers of...coated reticle blank. Thereafter, the pattern for a particular layer to be formed on a **semiconductor** wafer is transferred onto the reticle as for example by a laser pattern generator or...macro, contaminants can settle on the reticle which can interfere with pattern transference onto the **semiconductor** wafer.

It is therefore advantageous to prevent particles from adhering to reticles during reticle fabrication...

...the reticles, during transfer of the reticle from I 0 the reticle fab to the **semiconductor** fab and during usage of the reticle in the **semiconductor** fab.

During **semiconductor** and reticle fabrication, it is known to store such WO 02/095542 PCT/US02/21861...RNENTION
It is therefore an advantage of the present invention to provide a modular 0 **reticle management system** wherein the **storage** capacity and footprint ofthe system ...sorter coupled to one or more stockers that allow a customized configuration of the overall **reticle management system** . The **stockers** may be bare reticle stockers, closed container reticle stockers, or both. In embodiments ofthe present invention, the **reticle management system** includes between one and six individual bare reticle 5 stockers and/or closed container stockers ...it is understood that the present invention may operate with other workpieces, including for example, **semiconductor** wafers and flat panel displays. Preferred embodiments of the present invention comply with and allow...the controller I I 0 may be located to
a side or remotely from the **reticle management system** 100 in alternative
embodiments. The ability to locate the controller 1 1 0 at different...

...level of flexibility to the present invention and further allows a manufacturer to customize the **reticle management system** 1 00 as desired. Moreover, as all of the electronics and power components are centralized...bare reticle stockers 102 may be quickly and easily added to or removed from the **reticle management system** 100. Upon addition of a new bare reticle **stocker** 102 to the **management system** 100, a technician can reconfigure the controller 1 1 0 via the graphical user interface...two stockers on each of three sides of sorter 101, for manufacturers requiring large reticle **storage** capacities. A **reticle management system** configured with six bare reticle stockers is shown in Fig. 8. Alternatively, where only a small reticle storage space is needed, the **reticle management system** may be configured with only a single bare reticle stocker 102. It is contemplated that the **reticle management system** may be larger or smaller than that shown in Fig. 1 so as to hold...

...or less than two bare reticle stockers per side. Alternatively, it is contemplated that the **reticle management system** 100 may have a footprint other than a square or rectangular configuration so as to...

Claim
... reticle management system as recited in claim 1, wherein said one or more bare reticle **stockers** in the **reticle management system** may be varied between one and six.

4 A reticle management system as recited in...reticle management system as recited in claim 8, wherein said one or
more bare reticle **stockers** in the **reticle management system** may be varied between one and six.

10 A reticle management system as recited in...the reticle 1 5 management system operating with a variable number of closed container reticle **stockers** .

14 A **reticle management system** , comprising:
a **reticle** sorter; and
at least one stocker from a group of stockers comprising a bare reticle...

7/3,K/9 (Item 6 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00895323 **Image available**

DEFECT KNOWLEDGE LIBRARY

BIBLIOTHEQUE DE CONNAISSANCES DE DEFAUTS

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Patent and Priority Information (Country, Number, Date):
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Application: WO 2001US31028 20011002 (PCT/WO US0131028)
Priority Application: US 2000237297 20001002; US 2001905609 20010713
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Publication Language: English
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Fulltext Word Count: 16046
Fulltext Availability:
Detailed Description

English Abstract
...apparatus for creating a defect knowledge library containing case study information of wafer defects on **semiconductor** wafers. The method comprises creating a database entry that contains a case study of a...

Detailed Description
... invention generally relates to a method or associated apparatus for performing defect analysis in a **semiconductor** wafer processing system. More particularly, the invention relates to a database that stores images and other information relating to defects on **semiconductor** wafers.

5
Description of the Related Art
Semiconductor wafers are prone to defects that occur during processing.

Defects may occur at any stage of the processing of the wafers as **integrated circuits** are formed thereupon. Generally each fabricator of **integrated circuits** maintains a database of the causes of defects that occur on a regular basis. If...

...the solution to be to execute a cleaning cycle for the particular chamber.

The various **integrated circuit** fabricators develop their own proprietary
databases of defect information. As such, substantial funds are expended ...

...need in the art for a method for pooling the confidential defect information of multiple **integrated circuit** fabricators. This defect information could be accessed by various fabricators in a manner that would...

...present invention is a method and.apparatus for creating a database comprising images and other **semiconductor wafer** defect information. The **database** is stored in a server having a plurality of clients connected thereto. The images and other information are **supplied** to the **database** from the clients. The clients collect the information and images from local metrology cells, then 186 stores **semiconductor** wafer defect case histories in a DKL database 190. The case history information is 1 5 stored, organized and accessed by DKL software 188. Such **semiconductor** wafer defect case histories can be accessed by remote users (clients 104) of the defect...

...system (or to an operator located at the wafer processing system).

The term "wafer" includes **semiconductor** wafers or some other form of substrate upon which sequential process steps are performed. The...or process that facilitates the identification of defects on a wafer or defects in an **integrated circuit** formed on the wafer (generally referred to herein as defects or wafer defects interchangeably).

KLA...

7/3,K/11 (Item 8 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00848452 **Image available**
RETICLE MANAGEMENT SYSTEM
SYSTEME DE GESTION DE RETICULES
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Patent: WO 200182055 A1 20011101 (WO 0182055)
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(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
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Publication Language: English
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Detailed Description
Claims

English Abstract
A **reticle management system** (100) is disclosed that provides data storage and retrieval of data associated with each reticle...

...and certain system attributes and also for the efficient movement and storage of reticles and **reticle** carriers. The **reticle management system** includes a **reticle** management controller, a central **reticle database** , and one or more reticle stockers (102,104,106,108) that include a **stocker** controller, a **stocker database** , and a **stocker** unit.
Detailed Description
... N/A
BACKGROUND OF THE INVENTION
Lithography represents over 35% of the cost of manufacturing **integrated circuits** . Because this is a significant portion of the cost of an **integrated circuit** , reducing the costs associated with lithography and increasing the efficiency of the lithography process are important to lowering the overall costs associated with

the manufacture of **integrated circuits** .

Presently, reticles that are used as masks in the lithography process are manually handled during...

...various reticles and to manage the various reticles accordingly.

BRIEF SUMMARY OF THE INVENTION

A **reticle management system** is disclosed that provides data storage and retrieval of data associated with each reticle, reticle...

...and certain system attributes and also for the efficient movement and storage of reticles and **reticle** carriers. The **reticle management system** includes a **reticle** management controller, a central **reticle database** , and one or more reticle stockers that include a **stocker** controller, a **stocker database** , and a **stocker** unit. The reticle management controller is coupled to the central **reticle database** and each of the stocker controllers. Each stocker controller collects data on the reticles, reticle...

...both, that are stored within the associated stocker unit and stores this data in the **stocker database** . The **reticle** management controller retrieves the data in each **stocker database** via the associated **stocker** controller and stores this data in central **reticle database** . In addition, data attributes for the system, and the reticle carriers within the system may also be stored in the central **reticle database** .

The **reticle management system** may be coupled to a reticle movement system and can allow both user input move...

...in conjunction with the drawings of which.

Fig. 1 is a schematic representation of a **semiconductor** wafer processing facility; Fig. 2 is a block diagram of a reticle management system in...

...used herein, a reticle is a photo mask or negative used in lithographic processing of **semiconductor** wafers. A reticle carrier is a material transport vehicle or device that is designed to...

...reticle loaded onto a reticle carrier.

Fig. 1 depicts an exemplary schematic view of a **semiconductor** manufacturing facility 100. The facility includes a plurality of bays 101, 103, 105, and 107...

...has at least one stocker 102, 1041, 106, and 108, respectively, that contains lithographic reticles, **semiconductor** wafers, or both. In addition, each of the plurality of bays 101, 103, 105, and...

...136-142,, and 144-150, respectively, that are used to process the wafers in the **semiconductor** manufacturing process. it should be understood that the schematic representation depicted in Fig. 1 is...by the stocker to the RMS server that is used to is populate the RMS **database** . As new **reticles** or carriers are added to the system,, the stocker containing the new

reticle or carrier will provide the necessary data to the RMS controller for **storage** in the RMS **database** .

The user may also cancel any user initiated command prior the beginning of execution of...

Claim

1 An apparatus for managing data corresponding to a plurality of reticles in a **semiconductor** manufacturing system including a plurality of processing stages, the apparatus comprising:
a central reticle database...

...the reticle management controller configured and arranged to store and retrieve data from the central **reticle database** ;
a **stocker** including a **stocker** controller, a **stocker database** , and a plurality of storage locations configured and arranged to store at least one of the plurality of reticles, the stocker controller coupled to the **stocker database** , the **stocker** controller configured and arranged to store at least a portion of the plurality data corresponding...

...one of the plurality of reticles stored within the plurality of storage locations within the **stocker database** ; and
the **reticle** management controller coupled to the stocker controller, the reticle management controller configured and arranged to...

...of storage locations and to store the at least a portion of data within the **stocker database** ; and
the **reticle** management controller coupled to each of the plurality of stocker controllers, the reticle management controller...the plurality of stockers.

16 An apparatus for managing a plurality of reticles in a **semiconductor** manufacturing system including a plurality of processing stages, the apparatus comprising:
a central **reticle database** configured and arranged to store data corresponding to each of the plurality of reticles;
a reticle management controller coupled to the central **reticle database** , the **reticle** management controller configured and arranged to store and retrieve data from the central **database** ;
a **stocker** unit including a **stocker** controller, a **stocker database** , and a plurality of storage locations configured and arranged to store at least one of...

...of storage locations and to store the at least a portion of data within the **stocker database** ;
the **reticle** management controller coupled to the stocker controller, the reticle management controller configured and arranged to...

...unit.

20 An apparatus for managing data corresponding to a plurality of reticles in a **semiconductor** manufacturing system including a plurality of processing stages, the apparatus comprising:
a central reticle database...

7/3,K/12 (Item 9 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00824079 **Image available**

RETICLE STOCKING AND SORTING MANAGEMENT SYSTEM
SYSTEME DE GESTION DE STOCKAGE ET DE TRI DE RETICULES

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Patent and Priority Information (Country, Number, Date):
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Fulltext Availability:
Detailed Description

English Abstract
A system and method for stocking and sorting reticles used in a **semiconductor** fabrication facility, the facility having a material handling system that presents a reticle to a photolithography process area. In an example embodiment of the **reticle management system** , a **reticle storage** system and a reticle sorting apparatus are coupled to a host system that is adapted...

...management directives into the reticle flow plan in the manufacturing process. The result is a **reticle management system** that is flexible enough to manage a finite number of reticles and pods in minimizing...

Detailed Description
... system and method for managing reticles and reticle stocking locations as part of an entire **semiconductor** processing system.

Background Art
0 A conventional **semiconductor** fabrication plant typically includes multiple fabrication areas or bays interconnected by a path, such as...

...belt. Each bay generally includes the requisite fabrication tools (interconnected by a subpath) to process **semiconductor** wafers for a particular purpose, such as photolithography, chemical-mechanical polishing, or chemical vapor deposition. Material stockers or stocking tools generally are located about the plant and store **semiconductor** wafers waiting to be 5 processed. The wafers are typically stored in containers, such as...

...underlying wafer are then sub.ected to further processing.

0 Depending on the type of **IC** device being manufactured, the wafer may be subjected to the photolithography process several times as layers are formed successively over prior layers to ultimately form the **semiconductor** device. To perform the various photolithography processes, a **semiconductor** plant has a photolithography area that has a number of steppers that utilize an entire...

...above, and other needs in connection with improving efficiencies of reticle stocking and sorting processes.

Semiconductor fabrication facilities have material handling systems that manage production/test wafers as well as empty...invention in connection with the accompanying drawings, in which.

0 FIG. I illustrates an exemplary **semiconductor** fabrication facility in accordance with one
embodiment of the invention; and
FIG. 2 illustrates a...

...is generally directed to a system and method for managing and handling masks in an **IC** manufacturing envirom-nent, particularly where an automated material handling system is used. It has been discovered that the present invention is particularly suited for stocking and sorting reticles in a **semiconductor** fabrication facility such that delivery time of the 5 reticle is minimized while the system...
...embodiments that follow.

C
3
Moreover, while the exemplary embodiment is used primarily in a **semiconductor** wafer processing facility. it should be appreciated that the invention is not necessarily so limited...

...steppers 120. The steppers generally use a number of different reticles for fabricating layers of **semiconductor** wafers. The invention is however not necessarily limited to the use of photolithography steppers. but...the present invention is applicable to a number of techniques for managing masks in an **integrated circuits** manufacturing system. Accordingly, the present invention should not be considered limited to the particular examples...

...For instance. while the management of reticles in an automated material handling systems of a **semiconductor** facility is illustrated. the invention extends to cover other the management of different types of...
?

t s13/3,k/1,2,7,8,9,17,18

13/3,K/1 (Item 1 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

01346350
Wafer fabrication data acquisition and management systems
Systeme zur Verwaltung und Erfassung von Waferherstellungsdaten
Systemes de gestion et d'acquisition de donnees de fabrication de galettes
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PATENT (CC, No, Kind, Date): EP 1150187 A2 011031 (Basic)
APPLICATION (CC, No, Date): EP 2001104512 010302;
PRIORITY (CC, No, Date): US 561440 000428
DESIGNATED STATES: AT; BE; CH; CY; DE; DK; ES; FI; FR; GB; GR; IE; IT; LI; LU; MC; NL; PT; SE; TR
EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI
INTERNATIONAL PATENT CLASS: G05B-019/042; H01L-029/00
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NOTE:
Figure number on first page: 8

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	200144	1900
SPEC A	(English)	200144	10552
Total word count - document A			12452
Total word count - document B			0
Total word count - documents A + B			12452

...ABSTRACT A2
The present invention provides a **semiconductor** processing device (800) including a tool (802) having one or more sensors, a primary data ...

...SPECIFICATION A2

FIELD OF THE INVENTION
The present invention relates to devices, techniques and methods for **semiconductor** processing.

BACKGROUND OF THE INVENTION
A **semiconductor** device such as an **IC** (**integrated circuit**) generally has electronic circuit elements such as transistors, diodes and

,resistors fabricated integrally on a single body of **semiconductor** material. The various circuit elements are connected through conductive connectors to form a complete circuit which can contain millions of individual circuit elements. **Integrated circuits** are typically fabricated from **semiconductor** wafers in a process consisting of a sequence of processing steps. This process, usually referred...

...deposition, planarization and cleaning.

A summary of an aluminum gate PMOS (p-channel metal oxide **semiconductor** transistor) wafer fab process 40 is schematically shown in FIG. 1, illustrating major processing steps 41 through 73, as described in W.R. Runyan et al., **Semiconductor Integrated Circuit** Processing Technology, Addison-Wesley Publ. Comp. Inc., p.48, 1994. Each of these major processing...

...Pat. No. 5,236,868 (J. Nulman, 1993) which employs a vacuum apparatus having a **central** chamber and four processing chambers. A wafer handling robot in the **central** chamber has access to the interior of each the processing chambers in order to transfer wafers from the **central** chamber into each of the chambers while keeping the wafers in a vacuum environment. In...

...source to the deposition substrate, as described more fully in the '297 patent.

Advances in **semiconductor** materials, processing and test techniques have resulted in reducing the overall size of the **IC** circuit elements, while increasing their number on a single body. This requires a high degree...

...is an error in the overlay or alignment of etch masks for interconnects in adjacent **IC** layers, the resulting interconnects are not in their proper design location. This can result in...to maintain the process within these limits, see for example R. Zorich, Handbook Of Quality **Integrated Circuit** Manufacturing, Academic Press Inc., pp. 464-498, 1991. SPC and SQC methodologies suitable for a...

...472-478, 1997.

It is known to acquire processing data from multiple sensors within a **semiconductor** processing system and to utilize the acquired data for process monitoring, see for example U...

...or more signals or parameters, thus improving detection of a decision threshold.

A unit of **semiconductor** manufacturing equipment, such as a wafer fab tool, commonly employs an on-board computer to...

...is well known to those of ordinary skill in the art that the functions of **semiconductor** manufacturing equipment, including for example a wafer fab, can be defined in basic equipment states...

...96, Standard For Definition And Measurement Of Equipment Reliability, Availabilily, And Maintainability (RAM), published by **Semiconductor** Equipment and Materials International (SEMI), pp. 1-23, 1996. The **semiconductor** industry typically uses these six equipment states to measure and express equipment RAM (reliability availability...3-5 provide a basis for communicating and evaluating RAM related equipment information in the **semiconductor** industry. RAM related equipment information includes topics which are well known to those of ordinary...

...in the dependent claims.

The present novel techniques for data acquisition and management systems of **semiconductor** processing devices and wafer fabs provide the needed improvement in data acquisition, process control, quality, yield and cost reduction.

In one embodiment of the present invention, a **semiconductor** fabricating tool and processing methods are provided wherein the tool includes a primary communication port...

...port. The facility additionally includes a host database and host computer as well as a **data base management system** and **wafer** fab management software. Tool operating instructions are executed employing legacy software communicating via the primary...

...In yet another embodiment of the present invention, a computer executable process for operating a **wafer** fab **management system** is provided. The system derives a model for the system by defining wafer fabrication data...

...data structures.

In still another embodiment of the present invention a network distributed database for **semiconductor** fabricating is provided utilizing a plurality of **semiconductor** processing devices each having a tool including a primary and secondary data communication port. A network is provided for interconnecting the plurality of **semiconductor** devices ...organized in relational tables, are adapted for being accessed by one or more applications for **semiconductor** fabricating. For example, a recipe manager application can access a recipe manager relational table or...

...stack chart illustrated in FIG. 3.

FIG. 6 is a block diagram schematically illustrating a **semiconductor** processing device of the present invention.

FIG. 7 is a block diagram schematically illustrating another **semiconductor** processing device of the present invention.

FIG. 8 is a block diagram schematically illustrating an additional **semiconductor** processing device of the present invention.

FIG. 9 is a block diagram schematically illustrating a...

...of the present invention.

FIG. 10 is a block diagram schematically showing a networked, distributed **database management system** for managing a **wafer** fab **management system** of the present invention.

FIG. 11 is a block diagram illustrating hierarchical relationships between data...

...as all equivalents.

One embodiment of the invention, schematically illustrated in FIG. 6, shows a **semiconductor** processing device 600, employing an EDAS (enhanced data acquisition system) of the present invention. The novel EDAS is adapted for monitoring, i.e. observing, analyzing and reporting, **semiconductor** wafer or **IC** (**integrated circuit**) fabricating or processing tools, hereinafter referred to as tools. These tools include wafer fab chambers...

...acquired data, data structures or information.

Tool 610, as depicted in FIG. 6, includes such **controllers** (not shown) and inputs as are necessary to produce the desired wafer or **IC** structures, for example microprocessors including on-board computers, computer operated software as well as mechanical/electrical **controllers** including switches and electrical circuits employing for example a variable resistor such as a potentiometer. These **controllers** operate or control various tool processes and operational functions such as gas flow and wafer...

...optical components and conventional wireless communication techniques.

Information processing and analyzing environment 624 of novel **semiconductor** processing device 600, shown in FIG. 6, utilizes methodologies such as are well known to...

...the art, to determine process control limits meeting the design and yield criteria for producing **semiconductor** wafers and **IC** structures. The control limits are statistically derived using one or more processing and/or in...

...the '989 patent for measuring the sheet resistance of an electrically

conductive film on a **semiconductor** substrate in-situ, while maintaining the substrate within the vacuum environment of the **semiconductor** process apparatus. The data which are obtained from the process while running in control, i...

...were used to determine the control limits.

Information processing and analyzing environment 624 of novel **semiconductor** processing device 600 (FIG. 6) is adapted for comparing real time data with historical data...provided by a host computer 640 (FIG. 6). It will also be understood that novel **semiconductor** processing device 600 includes a novel product or a novel apparatus comprising one or more...

...port 646.

Another embodiment of the present invention, schematically illustrated in FIG. 7, shows a **semiconductor** processing device 700 of the present invention. This device includes a tool 702 having one...

...reporting environment 636 of device 600, shown in FIG. 6.

In a specific embodiment, novel **semiconductor** processing device 700 is utilized to determine the endpoint of a wafer etching process. Upon... and the novel EDAS functions are combined, as schematically illustrated in FIG. 8, depicting a **semiconductor** processing device 800. Device 800 includes a tool 802 having one or more sensors (not...

...and the operation of tool 802 and data acquisition subsystem 808 using familiar interface devices. **Semiconductor** processing device 800 also includes a peripheral device 834, such as a pump or a...

...a network.

A further embodiment of the present invention provides a network system 900 of **semiconductor** processing devices. Network system 900, schematically illustrated in FIG. 9, includes a plurality of **semiconductor** processing devices exemplified by devices 902, 904 and 906, a DBMS (database management system) 908, and a network 910 interconnecting the separate **semiconductor** manufacturing devices and the DBMS. The resulting system forms a network distributed database that includes...

...embodiment of system 900, DBMS 908 is configured as a network server and the individual **semiconductor** processing devices 902, 904, and 906 are configures as network clients. **Semiconductor** processing devices suitable for use in the present invention include **semiconductor** processing devices 600, 700 and 800, illustrated in FIGS. 6, 7 and 8 respectively.

Another...

...one or more sensors (not shown) for providing EDAS data. System 1000 also includes a **database management system** 1024, **wafer** fab management software 1026, a network interface 1028, a network 1030, EDAS tool subsystems 1032...added to the legacy system of wafer fab component 1002, shown in FIG. 10, through **database management system** 1024 and **wafer** fab management software 1026 that are integrated with host computer 1020 and host DB 1022...

...a specific embodiment, host computer 1020 is a work station having one or more mass **storage** devices such as host **DB** 1022. In this specific embodiment, **database** management 1024, **wafer** fab management software 1026, and network interface 1028 features reside within work station 1020, while the database and data structures reside partly on host **DB** 1022 and partly on mass **storage** devices 1066-1072 of tool subsystems 1032-1038 As described above, databases of system 1000 are synchronized to transfer copies of the duplicated information from **wafer** fab 1002 to **database** 1024. The present invention includes EDAS data, including sensor data, acquisition via secondary ports 1042...

...implements each EDAS tool subsystem 1032 - 1038 as a network client. In

other specific embodiments, **wafer** fab **management system** 1000 includes one or more non-tool client computers 1040 that are used to extend...

...database 1022 and EDAS tool subsystems 1032-1038.
In another specific embodiment of novel fab **management system** 1000 (FIG. 10), **wafer** fab management software 1026 is partitioned between host work station 1020 and the individual EDAS...
...via a more limited network connection such as network 1030.
The acquired EDAS data of **wafer** fab **management system** 1000 is maintained within individual EDAS tool subsystems 1032 - 1038, wherein the acquired EDAS information of each tool is stored on the tool subsystem mass **storage** devices 1066-1072. The **database** management function 1024 is also partitioned between the host work station 1020 and the tool...

...tool subsystems' mass storage device 1066-1072. The resulting distribution of portions of the system **database** among the host computer mass **storage** 1022 and the tool subsystems' mass storage devices 1066-1072 defines a networked, distributed database...

...inventories available to the user at any time via a user interface using the distributed **database** of **wafer** fab **management system** 1000.
Wafer fab management software 1026 implements a user interface feature permitting management system 1000 to be...

...to appropriate user inputs for modifying the system configuration.
In a specific embodiment of novel **wafer** fab **management system** 1000, the **wafer** fab management software includes a set of security rules governing user access to the sensor...tools of a wafer fabrication system. An example of a computer executable process for a **wafer** fab includes the combination of **DBMS** 1024, **wafer** fab management software 1026, network interface 1028 and host computer 1020 of device 1000, depicted...

...structure the entire set of control system data 1101 (FIG. 11) as a database. A **database** , when viewed as a data **storage** repository, includes an entire set of system data, their relationships and constraints on them that...present invention, schematically illustrated in FIG. 12, shows a computer implemented control system 1200 for **semiconductor** fabricating. This system includes a database 1202, a database management system (DBMS) 1204, a data...

...1206, EDAS tool subsystems 1208, 1210, 1212 (similar to EDAS tool subsystems 1032-1038 of **wafer** fab **management system** 1000, illustrated in FIG. 10, a tool configuration application 1214, a user configuration application 1216...

...the old by means of SECS II protocol messages. The applications are adapted for controlling **semiconductor** manufacturing.
The use of a database and database applications provide novel properties and features to...wafer fabrication system to obtain a desired result, e.g., the production of a specific **integrated circuit** type. Control of the system is achieved in one of two alternative ways. In a...

...902 - 906. In another specific embodiment of the novel computer executable process for operating a **wafer** fabrication system the **database management system** 908 is assigned total responsibility for insuring that all data structures for the model are...

...CLAIMS A2
1. A **semiconductor** processing device including a **semiconductor** processing tool (610, 702, 802), the device comprising:
a first data communication port (612, 730...

...642, 615; 705, 733), combined MES and enhanced data acquisition system input devices (826), and **databases** .

14. A **wafer** fabrication facility (1000) comprising:
a plurality of tools (1004-1010);
each of the plurality of...

...1010);
a database management system (1024) integrated with the host computer (1020) and the host **database** (1022); and
wafer fab management software integrated with the host computer (1020) and the host database (1022).
16...

...or more applications communicate with the database management system.
18. A network distributed database for **semiconductor** fabricating, the distributed **database** comprising:
a **wafer** fabrication facility according to any of the claims 15, 16 or 17; and
a network (1030)interconnecting the plurality of **semiconductor** tools (1012-1018) and the database management system (1024).
19. A method for processing data...

...method comprising:
integrating a database management system (1024) with the host computer (1020) and host **database** (1022);
integrating **wafer** fab management software with the host computer and host
database; synchronizing duplicate values of operating...of claim 19, 20 or 22, additionally comprising a network interface (1028) for interfacing the **wafer** fab management software and **database management system** (1024) with each tool client (1058-1064) of each tool subsystem (1032-1038, 1208-1212...

...a maximum baud rate of about 38400.
37. A computer executable process for operating a **wafer** fabrication **management system** (1000) comprising:
deriving a model for the system by defining wafer fabrication data structures and...or more of the tables are adapted for being accessed by an application for controlling **semiconductor** fabricating, wherein the application is selected from the group consisting of tool configuration, user configuration...

13/3,K/2 (Item 2 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00312441
Computer aided discrete traveler system for integrated control.
Computerunterstutztes diskretes Bewegungssystem fur integrierte Steuerung.
Systeme de deplacement discret assiste par ordinateur pour commande integree.
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PATENT (CC, No, Kind, Date): EP 292236 A2 881123 (Basic)
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EP 292236 B1 930421
APPLICATION (CC, No, Date): EP 88304451 880517;

PRIORITY (CC, No, Date): US 54212 870518
DESIGNATED STATES: DE; GB; NL
INTERNATIONAL PATENT CLASS: H01L-021/00; B25J-009/00;
ABSTRACT WORD COUNT: 88

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	EPBBF1	962
CLAIMS B	(German)	EPBBF1	989
CLAIMS B	(French)	EPBBF1	1150
SPEC B	(English)	EPBBF1	6295
Total word count - document A			0
Total word count - document B			9396
Total word count - documents A + B			9396

...ABSTRACT A2
Disclosed is a system mounted with a transportable container for carrying articles such as **semiconductor** wafers which comprises a non-volatile memory used to store the identity, status and history...

...SPECIFICATION B1
The present invention relates to standardized mechanical interface systems for reducing particle contamination of **semiconductor** wafers during **semiconductor** processing. More particularly, the **present** invention relates **to** an apparatus for information processing in standard mechanical interface systems.
A standardized mechanical interface (SMIF...

...filtering and other techniques attempts are made to remove particles which may cause contamination on **semiconductor** wafer surfaces. The SMIF concept is one **way** which has come under consideration for improving the processing environment over that available in clean...

...an apparatus for transporting articles between work stations comprising:
at least one transportable container for **the** articles, said container being adapted to be mounted at at least one of said work...

...is mounted thereat;
selection means for selecting between respective sensing means of said plurality; and
central processor means coupled to said selection means for receiving digital information from and for providing...engaging means, whether a cassette of wafers is within the container or not, whether the **container is in** its opened or closed condition, and other conditions which may be relevant to the **particular processing sequence** being conducted.
Fig. 1 shows a perspective view of a SMIF system positioned adjacent processing equipment.
Fig. 2 is a schematic representation of **a** SMIF system employing the present invention.
Fig. 3A **and** 3B are circuit diagrams of one embodiment of the present invention.
Fig. 4 is an...

...power supply according to the present invention.
Fig. 6 is a schematic representation of the **mounting** relationship of apparatus according to the present invention.
Fig. 7 is a **block** diagram of a system included on the transportable container in one embodiment of the present...

...of the processing system in accordance with the present invention.
Fig. 10 is an alternative **flow** chart for substitution for a portion of the flow chart of Fig. 9.
Fig. 11...

...invention.

Fig. 12 is a perspective view of a tray and transportable container of the **inventory management system** in accordance with the present invention.

Fig. 13 is a block **diagram** of an **inventory management system** in accordance with the invention.

With reference to the drawings, a detailed description of the present invention is provided.

In Fig. 1, a **semiconductor** wafer processing station 100 is shown. A given **semiconductor** manufacturing process may include any number of processing stations such as the station 100 shown...

...materials, the alignment of masks for exposing photo resist materials, the deposition of materials on **semiconductor** wafers, and so forth.

Fig. 1 shows a transportable container 10 for **semiconductor** wafers, or other articles to be processed, mounted on the processing station 100. The transportable...

...transportable container 10 is adapted for containing a cartridge 31 for holding a plurality of **semiconductor** wafers 32. The cartridge 31 is lowered into the processing station 100 without exposure to...

...the processing station 100. The data processor 20 may include a display 21 such as **an** LED or liquid crystal display. Also, the data processing 20 may include a keyboard 22...

...card 40 attached to the container 10. The data stored in the data card 40 **is** communicated to the means 50 on the processing station 100 for communicating with the data...

...and fully engaged, the port 70 on the canopy 30 through which the cartridge of **semiconductor** wafers is lowered, is aligned with the transportable container 10. The data card 40 is...

...card 40. The communicating means 50 is connected over communicating line 51 to the process **controller** 20 on the processing station 100.

Fig. 3A illustrates a circuit for mounting on the...being carried out and the characteristics of articles being transported in the transportable container 10.

The plurality of input/output devices **153 includes a** transmitter 163 and a receiver **164** such as the light emitting diode 44 and photosensitive transistor 52 discussed with reference to Figs. 4 and 6. The transmitter 163 and receiver 164 may be of other varieties **of phototransistors and** photodetectors as **suited** to the particular use required. Further, the transmitter and receiver may be comprised of a...

...time for the articles contained in the transportable container 10.

In accordance with the present **invention , the transportable** container 10 with the data card 40 attached to it can be used in conjunction...

...form a novel distributed processing system. Once such distributed processing system is used to fabricate **semiconductor integrated circuits** . The fabrication of **semiconductor integrated circuits** typically **involves the processing** of **semiconductor** wafers using **a** variety of discrete processing operations using a corresponding variety of work stations.

For example, the processing operations and corresponding work stations involved in the fabrication **of a semiconductor integrated circuit** from a **semiconductor** wafer might include the following operations and work stations. A resist is applied to the...

...at a second work station. A circuit pattern is exposed onto the resist at a **third work** station. The circuit pattern is developed at a fourth work station. The width of one...

...few of a large variety of possible processing steps and work stations.

In a given **semiconductor integrated circuit** processing

environment, there may be a variety of batches of wafers simultaneously undergoing fabrication. Each batch **may be enclosed** within a different transportable container 10 or group of containers each with its own associated...

...undergo different operations at different work stations so as to ultimately produce different types of **semiconductor integrated circuits** . Alternatively, different batches of **semiconductor** wafers may use the same work stations, but may be processed somewhat differently by the work stations aso as to ultimately produce different types of **semiconductor integrated circuits** . For example, the resists of two batches of wafers both might be etched at the...

...Additionally, the nature of the processing operations to be performed in the course of fabricating **integrated circuits** from a batch of wafers may depend upon the outcome of earlier processing steps. For...of the present invention for the control of complex processing operations like the manufacture of **semiconductor integrated circuits** .

Referring to the drawing of Fig. 1, it will be appreciated that the work station...

...card 40 can engage in two-way communication, through transmitter 104 and receiver 106, with **means 50** . **Referring** once again to Fig. 9, the local 20 is in electronic communication with local transfer...

...with reference to an exemplary manufacturing operation and with particular reference to the fabrication of **semiconductor integrated circuits** , but it should be appreciated that the system is applicable to other operations as well...

...Figs. 1 and 9, after the container 10 is engaged to the work station 100, **indicated as step** 402 in the flow chart of Fig. 9, the local 20 querries the **data** card 40 as to whether it is ready to exchange digital information, step 404. The...

...20 then requests that the card 40 identify itself and provide the current processing data, **step 414** . **In** response, the card 40 provides an identifying code. In a **semiconductor integrated circuit** manufacturing processing system, the card might also identify the lot number of the **semiconductor** wafers to be processed as well as the identity of the work station which is...

...what processing step is to be performed next, step 416. For example, the next processing **step** might be the exposing of a circuit pattern onto a resist at the third work...from the transportable container 10 to the work station 100, step 422. For example, in **semiconductor integrated circuit** fabrication, a cartridge 31 containing wafers 32 to be processed **is** lowered from the container 10 to the work station 100 via arms 306.

Next, the...

...processing operation to be performed by the work station might be to expose a circuit **pattern** onto a resist applied to a **semiconductor** wafer.

The local 20 informs the card that the transfer has been completed and that...

...the local transfer control processor 300 to imitate a transfer of the articles processed, the **semiconductor** wafers 32 for example, from the work station 100 back to the transportable container 10...

...record of the operation of exposing a circuit pattern onto a resist applied to a **semiconductor** wafer. The local 20 communicates the second history record to the card 40, step 442...

...40.

The first example will be explained with reference to Fig. 10 in which

there **is shown an** alternative flow chart path with can be substituted for steps 408-420 of the flow...

...hand, if the card 40 determines that it is operating properly, then the card 40 **requests** that the local 20 report its identity, step 504. In response, **the** local 20 identifies itself to the card 40, step 506. The card 40 then determines...

...in which a representative series of card operations and work station operations from an exemplary **semiconductor integrated circuit** fabrication process are shown. For the purposes of this example, the card 40 is assumed...

...width measured) + B (resist thickness). Where K, A and B are constant values, and the " **width** specified" refers to the specified width of a circuit trace, and "width measured" refers to...
...circuit trace, and "resist thickness" is the measured thickness of a resist applied to a **semiconductor** wafer.

The first processing step is **to apply a** resist to **semiconductor wafers** being processed, step 602. This step, **for** example, is performed at a first work station. The thickness of the resist is measured...

...examples, it will be appreciated that the card 40 advantageously can be used as part **of a distributed** processing system which does not require **centralized** control. Instead, a card 40 associated with a transportable container 10 containing articles to be...

...perform calculations necessary to properly process the articles.

The present invention also provides a novel **inventory management system** which advantageously can monitor the status of articles, such as **semiconductor** wafers for example, between processing operations.

Referring to the illustrative drawings of Fig. 12, there is shown a tray 630 including a recessed region 632 sized to **receive** a transportable container 10 having a data card 40 **mounted** on it as shown. The tray 630 includes a two-way communication means 50-1...

...means 50-1 such that the card 40 and the means 50-1 can engage **in two - way** communication with each other.

Referring now to the illustrative drawings of Fig. 13, there is shown in block diagram form a **inventory management system 637 which** includes a plurality of trays divided **into** respective groups of trays 630-1 through 630-N. Each respective individual tray is like...

...through 630-N is coupled by a respective control line 639-1 through 639-N **to** a multiplexer circuit 640-1 through 640-N. The respective multiplexers 640-1 through 640-N are coupled via control line 642, which for example can be an RS232 C **line** , to a **central** control processor 644.

In the presently preferred embodiment, the **central** control processor 644 comprises an IBM compatible personal computer. The multiplexers 630-1 through 630-N are coupled to one another in a **daisey** chain such that signals propagated along control line 642 proceed in a serial fashion from...

...trays 630-1 and 630-N are shown together with two associated multiplexer circuits 638- **1** through 638-N, it will be appreciated that a plurality of groups of trays and a corresponding plurality of groups of multiplexers can be included in the **inventory management system** 637.

In operation, a plurality of transportable containers 10 can be placed into the respective trays 630- **1 through 630** -N of the **inventory management system** 637. An operator can use the **central** control processor to ascertain, for example, the processing status of the contents of any container 10 received within any of **the** trays of the system 637.

More particularly, for example, in order to obtain information

regarding the contents of the container 10 shown in Fig. 12, the **central** control processor 644 instructs the respective multiplexer circuit (not shown) coupled to that that tray 630 to select that tray 630 and to couple it to the processor 644. The **central** control processor 644 sends digital signals to the selected tray 630 which cause two-way...

...way communication means 50-1 and the card 40. Through the two-way communication, the **central** control processor 644, for example, can ascertain the contents of the container 10, the processing...

...are scheduled to be performed in the future. Additionally, through such two-way communication, the **central** control processsor 644 can be used to reprogram the microcomputer 101 of the card 40...

...update or correct its real time clock.
Thus, it will be appreciated that the present **inventory management system** 637 advantageously can distribute, for example, the task of maintaining a history of the processing...

...schedule of future processing steps for the articles within respective transportable container 10. Consequently, the **central** control processor 644 is free from maintaining and managing such information. ...

...CLAIMS on said at least one transportable container for storing digital information processed by said microcomputer **means** ;
a plurality of respective sensing means, each adapted to have said at least one transportable container removably...

...is mounted thereat;
selection means for selecting between respective sensing means of said plurality; and
central processor means (644) coupled to said selection means for receiving digital information from and for...

...two-way communication means of respective sensor means of said plurality.
4. Apparatus according to **claim** 3 wherein each respective sensing means of said plurality further comprises respective receptacle means (632...

...to claim 6 wherein each respective selection circuit is adapted to couple selectively to said **central** processor (644) means any one respective sensing means of a respective group coupled thereto.
8. Apparatus according to claim 7 wherein each respective selection circuit comprises a multiplexor **circuit** (640).
9. Apparatus according to claim 6 wherein said respective selection circuits are coupled to one-another and to said **central** processor means such that said respective selection circuits form a hierarchy in which signals communicated between said respective **central** processor (644) and said respective selection circuits **respectively** proceed serially between said respective selection circuits.
10. Apparatus according to any of claims 1-9 wherein said **first** two-way communication means, said microcomputer means and said storage means are disposed on a...
...CLAIMS selection entre des moyens de detection respectifs de ladite pluralite ; et
un moyen de processeur **central** (644) couple audit moyen de selection pour en recevoir une information numerique et pour produire ...

...circuit de selection respectif est concu pour coupler de facon selective audit moyen de processeur **central** (644) un moyen de detection respectif quelconque d'un groupe respectif qui lui est couple...

...circuits de selection respectifs sont couples les uns aux autres et audit moyen de processeur **central** de telle sorte que lesdits circuits de selection respectifs forment une hierarchie dans laquelle

des signaux communiques entre ledit processeur **central** respectif (644) et lesdits circuits de selection respectifs se propagent respectivement en serie entre lesdits...

13/3,K/7 (Item 1 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

01074937 **Image available**
DIAGNOSTIC SYSTEM AND METHOD FOR INTEGRATED REMOTE TOOL ACCESS, DATA COLLECTION, AND CONTROL
SYSTEME ET PROCEDE DE DIAGNOSTIC DESTINES A L'ACCES D'OUTILS DISTANTS INTEGRE, COLLECTE ET COMMANDE DE DONNEES
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Fulltext Availability:
Detailed Description
Claims

English Abstract
...in a fabricator (FAB), the FAB having at least one automated manufacturing tool, a tool **controller** , and internal secure storage means; a second internal network in an original equipment manufacturer (OEM...

Detailed Description
... generated by the tools to different parties.

Related Art

[0002] High-technology manufacturing, such as **integrated circuit** (**IC**) manufacturing, often combines computerized manufacturing tools, tool operators, computer networks and other components to achieve an efficient, profitable manufacturing envirom-nent. The **IC** manufacturer often collects data from the manufacturing tools to keep watch on potential manufacturing problems and inefficiencies. The data collected are usually proprietary and often sensitive.

[0003] The **IC** manufacturers may need to provide the collected data to third party sources, especially, for example...

...the tool as well, to service the machines, and also for internal purposes.

[0004] Many **IC** manufacturing sites use different tools that are made by more than one OEM, often by...

...wants to keep the data from its tools confidential.

Venable Ref: 40005- 178417

[00051 Small **IC** manufacturing sites may not be readily accessible to the OEMs for service. It is usually not economical to maintain an on-site OEM representative for service, and such small **IC** manufacturing sites must often transport their service personnel to the site when service is needed...

...What is needed then is an improved method of sharing data remotely between OEMs and **IC** manufacturers, and other third-parties, that maintains data security for both the OEM and the **IC** manufacturer and that allows remote servicing of the tools.

Summary of the Invention

[0007] In...

...in a fabricator (FAB), the FAB having at least one automated manufacturing tool, a tool **controller** , and internal secure storage means; a second internal network in an original equipment manufacturer (OEM...

...to an OEM from a FAB, comprising the steps of. remotely connecting to an automated **semiconductor** manufacturing tool at a FAB; exposing SECs data from the tool; acting as the host...

...stored locally at the FAB for security.

[00035] Original equipment manufacturer (OEM): the manufacturer of **integrated circuit** manufacturing tools.

[00036] **Integrated circuit** manufacturer (ICM): an organization that manufactures **integrated circuits** (**IC**). ICMs have one or more FABs where the **ICs** are made. The **IC** -manufacturing tools are housed at ICM FABs.

[00037] Active session: A session that enables people...

...Linux, and Solaris operating environments.

[00054] Tool: A device for manufacturing some component of a **semiconductor** product. Tools typically reside in a highly secure and restricted area of the ICM facility...

...remote operation, and sensor data, and co-exists with existing FAB infrastructure (e.g. station **controller** , MES, etc.). A tool gateway server 312 is hot-swappable. Each tool gateway server 312...

...of the eCentre framework installed at a FAB site 102 housing one or more automated **semiconductor** manufacturing tools 402, which are each coupled

to a tool console server 404. The tool...

...For example, the eCentre server 412 can provide timestamping 424, business logic 426, messaging 428, **database** **storage** 430 and security 432. The client 422 also has access to a customer list 434...

...current session.

[00087] I. Session Management Methodology
[00088] With conventional ICM/OEM infrastructure, when a **semiconductor** tool is not
Venable Ref. 40005- 178417
[00090] A session represents a unit of work...embodiment of the present invention can also remotely manage the maintenance of software applications on **semiconductor** process tools. This allows the OEM clients to maintain remotely any software that is deployed...
...activities of an OEM client with minimal invasion. The eCentre session provides the capability of **centralized** control of the TELNET sessions.

[000113] F. XML Data Persistence Service
[000114] The system of the present invention can store **semiconductor** device data in a database, preferably in a keyed relational database. Tool data, in the...

...storage feature provides support that allows infonnation received from the tool to be sent to **storage** **database** . The software has the ability to assign classification levels to all tool parameters. Classified data ...

...outside the firewalls.

[000138] VI. Data Brokeriqg System
[000139] In the tuning and diagnosis of **semiconductor** equipment, it is necessary to have additional data about the wafers produced by the tool ...

...16, an exemplary embodiment of the
present invention includes a data brokering system 1602 for **semiconductor** wafer data within a FAB that allows for the request for data on a particular...

...as XML tool data 1606. The XML tool data 1606 and be stored in a **database** 1604. **Wafer** data from each tool 1610-1616 is then available to the other tools without providing...

Claim
... in a fabricator (FAB), said FAB having at least
one automated manufacturing tool, a tool **controller** , and internal secure
storage means;
a second internal network in an original equipment manufacturer (OEM...

...said OEM and said FAB in respective internal secure storage means and without using a **central** server on the external network.

3 The remote diagnostics system according to claim 1, wherein...

...to an OEM from a FAB, comprising the steps of
remotely connecting to an automated **semiconductor** manufacturing tool at a FAB;
exposing SECs data from said tool;
acting as the host...

...logical point-to-point connections between OEMs and FABs.

42 A data brokering system for **semiconductor** wafer data, comprising:
a FAB having at least one automated **semiconductor** wafer

manufacturing tool;
a plurality of OEMs, coupled to said FAB via a secure service net;
means for providing data about a **semiconductor** wafer manufactured by said tool to one of said OEMs without revealing information about said...

13/3,K/8 (Item 2 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

01073673 **Image available**
METHOD AND APPARATUS FOR MONITORING TOOL PERFORMANCE
PROCEDE ET APPAREIL DE CONTROLE DES PERFORMANCES D'UN OUTIL
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Patent and Priority Information (Country, Number, Date):
Patent: WO 2003103024 A2-A3 20031211 (WO 03103024)
Application: WO 2003US16882 20030528 (PCT/WO US03016882)
Priority Application: US 2002383619 20020529
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NI NO NZ OM PH PL PT RO RU SC SD SE SG SK SL TJ TM TN TR TT TZ UA UG US UZ VC VN YU ZA ZM ZW
(EP) AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IT LU MC NL PT RO SE SI SK TR
(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZM ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
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Fulltext Word Count: 17406

Fulltext Availability:
Detailed Description
Claims

English Abstract
A method and system for monitoring tool performance for processing tools in a **semiconductor** processing system. The **semiconductor** processing system includes a number of processing tools, a number of processing modules, a number...

Detailed Description
... reference in its entirety.

Field of the Invention
[0003] The present invention is related to **semiconductor** processing systems, particularly to **semiconductor** processing systems, which use Graphical User Interfaces (GUIs) to provide a monitoring system for tool status monitoring.

Background of the Invention
[0004] The cost and tempo of developing new **semiconductor** devices and building new manufacturing plants is continually increasing. Time-to-market for new **semiconductor** devices is critical for the profitability and success of a company. Consumers expect the latest...

...new machines
and processes is vital to meet the rapid shifts and changes in the **semiconductor** device market. **Semiconductor** manufacturing facilities also
face the challenge of maintaining and controlling hundreds of complex manufacturing processes and machines. Meanwhile, the **semiconductor** manufacturing facilities must allow major changes in devices and processes to be developed and implemented...

...initialize
manufacturing processes. A computer is ideal for these operations given the complexities in a **semiconductor** manufacturing plant from the reentrant wafer flows, critical processing steps, and maintainability of the processes...

...monitor process flows,
wafer states, and maintenance schedules. A variety of tools exist in a **semiconductor** manufacturing plant to complete these complicated steps from critical operations such as etching, to batch...

...of
the graphical user interface (GUI) of a control computer containing the installation software.

[0006] **Semiconductor** processing facilities require constant monitoring.

Processing conditions change over time with the slightest changes in...
...control is often performed by a number of different control systems having a variety of **controllers** . Some of the control systems may
have man-machine interfaces such as touch screens, while...

...aspect of the present invention provides a method of monitoring a processing tool in a **semiconductor** processing system, the method comprising: putting the processing tool into a first state; executing a ...

...present invention provides a tool status
monitoring system for monitoring a processing tool in a **semiconductor** processing system, the tool status monitoring system comprising: a plurality of sensors coupled to the...

...001 1] FIG. 1 shows a simplified block diagram of an advanced process controlled (APC) **semiconductor** manufacturing system in accordance with one embodiment of the present invention;
[0012] FIG.2showsasimplifiedviewofaflowdiagramforamonitoring process for processing tools in a **semiconductor** processing system in accordance with one embodiment of the present invention;
[0013] FIG.3showsanexemplaryrelationshipdiagramforstrategiesand plans...

...editor screen in accordance with the present invention.

Detailed Description of an Embodiment
[0036] In **semiconductor** manufacturing computers are generally used to control, monitor, and setup manufacturing processes. The embodiment described below provides a tool status monitoring system for a **semiconductor**
processing system. The system can include the monitoring of processing tools, processing modules (chambers), and...

...installing the system.

[0038] The tool status monitoring system components can operate on a tool **controller** . In addition, the tool status monitoring system software components

. can operate on the APC server...

...management.

[0040] FIG. 1 shows an exemplary block diagram of an APC system in a **semiconductor** manufacturing environment in accordance with one embodiment of the present invention. In the illustrated embodiment, **semiconductor** manufacturing environment 100 comprises at least one **semiconductor** processing tool I 1 0, multiple process modules 120, PM 1 through PM4, multiple sensors...

...aligning, temperature
control, lithography, integrated metrology (IM), optical data profiling (ODP), particle detection, and other **semiconductor** manufacturing processes.

[0043] Inoneembodiment,processingtooIllOcancompriseatoolagent (not shown), which can be a software process that runs...

...1, four process modules are shown, but this is not required for the invention. The **semiconductor** processing system can comprise any number of processing tools having any number of process modules...

...ODP sensor, an OES sensor, a VIP sensor, an analog sensor, and other types of **semiconductor** processing sensors including digital probes.
The APC data management applications can be used to collect...

...at least one of a.- VIP probe, OES sensor,
analog sensor, digital sensor, and a **semiconductor** processing sensor.

[0057] In one embodiment, a sensor interface can write the data points to ...

...the tables can be implemented in the IS 150 as
in-memory tables and in **database** 190 as persistent **storage** . The IS 150 can use Structured Query Language (SQL) for column and row creation as...

...by the IS 150. The contents of these tables can be posted to the relational **database** at the end of **wafer** processing.

[0064] In the illustrated embodiment shown in FIG. 1, a single client - 12
Mb...

...little input as possible. The GU[design
complies with the SEMI Human Interface Standard for **Semiconductor** Manufacturing Equipment (SEMI Draft Doc. #2783B) and with the SEMATECH Strategic Cell **Controller** (SCC) User-Interface Style Guide 1.0 (Technology Transfer 92061179A-ENG). Those skilled in the...

...for externally monitoring and for externally controlling
the tools, modules, sensors, and processes in a **semiconductor** processing
system. Alternately, the factory system 105 and/or an E-Diagnostics system
115canperformtoolstatusmonitoring. Forexample,ausercanaccessthe tool status monitoring system using a web based terminal that is coupled to the **semiconductor** processing system via factory system 105 and/or an EDiagnostics system 1 1 5.

[0077...tool status monitoring system is to use real-time and historical data to improve the **semiconductor** processing system's performance. To achieve this goal, potential problems can be predicted and
corrected...

...simplified view of a flow diagram for a monitoring process for processing tools in a **semiconductor** processing system in accordance with one embodiment of the present invention. The software and associated...

...can be performed for each production step being performed by a processing tool in the **semiconductor** processing system. A production step is an etching process, a deposition process, a diffusion process, a cleaning process, a measurement process, a transfer process, or other **semiconductor** manufacturing process. Strategies define what happens during a set of sequences on the processing tool...

...wafer currently being processed can be used. Alternately, the context of a substrate or other **semiconductor** product currently being processed can be used. When the context is determined, it can be...

...of a control strategy. In one case, a wafer-in event can trigger a system **controller** to look up the current context data, determine which strategy to run, and invoke the...

...When the data preprocessing plan is executed, time series data can be created from raw **data files** and saved in the **database ; wafer** summary data can be created from the time series data; and lot summary data can ...

...system flows through a set of steps between the real-time sensor collection and the **database storage** . Data collected can be sent to a "datahub" that can comprise a real-time memory...

...collection of other process modules. This reduces the amount of non-productive time for the **semiconductor** processing system.

[001 15] When a tool health control strategy comprises a judgment plan, the...

...wafer currently being processed can be used. Alternately, the context of a substrate or other **semiconductor** product currently being processed can be used. When the context is determined, it can be...

...least one analysis strategy. In one case, a wafer-out event can trigger a system **controller** to look up the current context data, determine which analysis strategies to run, and invoke...languages and can be sized and positioned differently.

[00156] An information panel may include the **central** portion of the screen, and the content can be screen-specific. In information panel 650 ...

...of navigation items, and a help item.

[001 62] An information panel may include the **central** portion of the screen, and the content can be screen-specific. In information panel 650 ...

...tool, a developer tool, a lithography tool, a metrology tool, an OIDP tool, or other **semiconductor** processing tool. In addition, selection means are available that allow a user to display a...

...tool, a developer tool, a lithography tool, a metrology tool, an ODP tool, or other **semiconductor** processing tool. In addition, selection means are available that allow a user to display a...

Claim
1 A method of monitoring a processing tool in a **semiconductor** processing system, the method comprising:
putting the processing tool into a first state;
executing a...

...threshold value.

25 A tool status monitoring system for monitoring a processing tool in a **semiconductor** processing system, the tool status monitoring system comprising:
a plurality of sensors coupled to the...

13/3,K/9 (Item 3 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

01010806 **Image available**
MONITORING AND CONTROLLING INDEPENDENT SYSTEMS IN A FACTORY
PROCEDE ET APPAREIL DE CONTROLE, DE SURVEILLANCE ET D'ANALYSE DE SYSTEMES INDEPENDANTS DANS UNE UNITE DE PRODUCTION
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ZITZMANN Oliver A, 35 Hill Road, Redding, CT 06896, US, US (Residence), DE (Nationality), (Designated only for: US)
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Patent and Priority Information (Country, Number, Date):
Patent: WO 200340882 A2-A3 20030515 (WO 0340882)
Application: WO 2002US35415 20021105 (PCT/WO US0235415)
Priority Application: US 2001337821 20011105
Designated States: AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GE GH HU IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG US UZ VN YU ZW
(EP) AT BE BG CH CY CZ DE DK EE ES FI FR GB GR IE IT LU MC NL PT SE SK TR
(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZM ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Publication Language: English
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Fulltext Word Count: 9011

Fulltext Availability:
Detailed Description
Claims

Detailed Description
... for the remote configuration, operation and monitoring of equipment within a factory, such as a **semiconductor** factory.

Background Art
A manufacturer typically coordinates a number of operational stages in order to manufacture and deliver finished goods to a customer. The

manufacture of **semiconductor** circuits, for example, typically involves a variety of component devices, often referred to as ancillary...

...gases, to or from various process tools that perforrn specific steps in the manufacture of **semiconductor** circuits.

The monitoring of component devices in a **semiconductor** factory is important, since the failure of any one of these component devices that are...fabrication process could easily suspend operations of a much larger unit or even the entire **semiconductor** factory. Since the cost of lost productivity has been estimated to vary fi-om $10...

...the fabrication process do not want to be responsible for suspending the operation of the **semiconductor** factory.

When a component used in the fabrication process fails, a service representative of the **semiconductor** factory must initially diagnose the cause of the failure to identify the vendor of the...device has been identified, the corresponding vendor typically sends a field service representative to the **semiconductor** factory to diagnose and remedy the particular problem. Once the field service representative arrives at the **semiconductor** factory, the field service representative performs a more detailed diagnostic procedure on the failing component...remedied. Thus, even when replacement parts are in stock, a failure can easily cause a **semiconductor** factory or a portion thereof to be down for two business days.

The **semiconductor** industry has recognized the need for **centralized** 0 monitoring of a **semiconductor** factory, and the ability to provide remote failure detection and diagnostics. International Sematech, a consortium of **semiconductor** industry companies, has published a specification that provides guidelines and requirements for implementing an e-Diagnostics system within a **semiconductor** factory. See, International Sematech, e-Diagnostics Guidebook, Version 1.4, September 3, 2002, incorporated by ...should enable bidirectional communication between a remote authorized field service representative and equipment in a **semiconductor** factory by means of a network or modem connection to thereby permit interactive configuration, operation customer (the **semiconductor** factory). In addition, the vendor can reduce the time and expense associated with sending field service representatives to the **semiconductor** factory. Even when it is necessary to send a field service representative to the **semiconductor** factory to perform a preventative maintenance task, the amount of required time is generally significantly ...a method and apparatus are disclosed for remotely configuring, operating and monitoring equipment in a **semiconductor** factory or another manufacturing facility. In addition, data from such equipment is collected and stored...

...subsequent analysis. According to one aspect of the invention, an interface to equipment in a **semiconductor** factory is provided that allows a remote user to establish a connection with the equipment...and protocols of different equipment manufacturers.

A web-based connection to remote equipment in a **semiconductor** factory allows a variety of diverse equipment systems to be accessed and controlled in a uniform manner over a network connection. In this manner, a **central** monitoring and control center provides a **centralized** collection point for equipment data, and permits decentralized distribution of persormel.
According to ...another aspect of the invention, the historical data that is collected from equipment in a **semiconductor** factory can be analyzed following a failure using pattern recognition techniques to identif@l patterns vendors in
a **semiconductor** factory and the collection and storage of data from such ancillary I 0 equipment also...

...there are a number of interrelated ancillary devices feeding a single

process tool in a **semiconductor** factory. A number of contributing events may cause a given failure and the present invention...is a schematic block diagram of a portion of a local area network with a semiconductor factory in accordance with the present invention; FIG. 3 illustrates the monitoring and control of various equipment devices
in a semiconductor factory in accordance with the present invention; FIG. 4 is a schematic block diagram of a central monitoring and control center incorporating features of the ...network environment in which the present invention can operate. As shown in FIG. 1, a **semiconductor** factory 200, discussed below in conjunction with FIGS. 2 and 3, is connected over a network 130, such as the Internet or Public Switched Telephone Network, to a **central** monitoring and control center 400, discussed below in conjunction with FIG. 4. The **semiconductor** factory 200 may include one or more local area networks employing well-known manufacturing equipment system (MES) connectivity techniques to connect the various equipment devices within the **semiconductor** factory 200. While the present invention is described in an exemplary **semiconductor** factory, the present invention can be applied to any manufacturing facility where multiple systems are and
monitoring of equipment in a **semiconductor** factory, as well as the collection and storage of data from such equipment in real time. The present invention provides an interface to equipment in a **semiconductor** factory that allows a remote user to establish a connection with the equipment in order...bi-directional communication between a remote authorized field service representative and the equipment in a **semiconductor** factory by means of a network or modem connection.

According to another aspect of the invention, the historical data that is collected from equipment in a **semiconductor** factory is analyzed following a failure using pattern recognition techniques to identify patterns in the...to occur.

The remote monitoring of ancillary equipment from a number of vendors in a **semiconductor** factory and the collection and storage of data from such ancillary equipment allows a multipoint...
...there are a number of interrelated ancillary devices feeding a single process tool in a **semiconductor** factory 200. There may be a number of contributing events that cause ...a variety of diverse equipment systems is obtained via network connections. In this manner, the **central** monitoring and control center 400 provides a **centralized** collection point for equipment data, and permits decentralized distribution of personnel.
1 5 FIG. 2 illustrates a local area network that may be employed in the **semiconductor** factory 200 to connect one or more equipment devices within the **semiconductor** factory 200. The local area network- may comprise an Ethernet, dedicated phone line, wireless modem...

...210 or related ancillary equipment (or both) is connected to one or more programmable logic **controllers** (PLCs) 220 that control the operation of the process tool 210 and related ancillary equipment...

...tool 210 or related ancillary equipment may be embodied as any component device within a **semiconductor** factory 200 that processes, measures, tests, or packages **semiconductor** material, such as tools, sensors, delivery and abatement systems, and control systems. The process tool 210 and programmable logic **controller** 220 generate data signals that are supplied to one or more network interface cards (NICs) 230.
The network interface cards 230 operate to query individual programmable logic **controllers** 220 for user-defined parameters. This data may be stored by the network interface card 230 or immediately forwarded over the network 130 to the **central** monitoring and control center 400.

According to one aspect of the invention, the network interface nation exchange with the local tools 210 (and related ancillary equipment) and the **central** monitoring and control center 400. The network interface cards 230 must translate between the diverse...format. The translated raw

data can then be loaded into an application server by the **central** monitoring and control center 400 for further processing.

In one embodiment, the network interface card...

...or integration (or both) of independent but related equipment systems and data sources within a **semiconductor** factory 200. The network interface cards 230 permit the **central** monitoring and control center 400 to gather raw data from diverse data sources. These data...

...code executed within the network interface card 230 translates data received from the programmable logic **controller** 220 associated with the data source into the desired uniform forniat.

In addition, the network...sensors that monitor the gas levels in a cabinet or in other locations of a **semiconductor** factory 200 for harmful conditions.

The network interface card 230 preferably secures the data that...

...the network interface card 230 is preferably configured to be able to communicate with the **central** monitoring and control center 400 or another authorized remote device through the firewall of the **semiconductor** factory 200, using known techniques. A firewall restricts access between a protected network and external...

...content of the packets.

As shown in FIG. 2, the local area network in a **semiconductor** factory 200 optionally includes a server 240 for interconnecting the various programmable logic **controllers** 220 and network interface cards 230 associated with each process tool 210.

The optional server 240 stores data and provides a **central** hub for communicating with the **central** monitoring and control center 400 over ...at least two communication ports, with a first communication port connected to the programmable logic **controller** 220 and a second communication port coupled to the server 240, or directly to thevia the programmable logic **controller** 220); (h) format the raw data in a desired uniform forinat; and (iii) provide the formatted data to the **central** monitoring and control center 400.

FIG. 3 illustrates the monitoring and control of various equipment devices in the **semiconductor** factory of FIG. '41 in accordance with the present invention. In particular, FIG. 3 illustrates...the embodiment shown in FIG. 3, the data storage device 350 is local to the **semiconductor** factory 200 and is managed, for example, by a chemical management interface 300. The chemical...functions 360 coordinate the transfer of data from the data storage device 350 to the **central** monitoring and control center 400 for further processing and analysis. In further variations, the data...

...of the server 240 (FIG. 2) or the data can be immediately forwarded to the **central** monitoring and control center 400 for processing.
FIG. 4 is a block diagram illustrating an exemplary **central** monitoring and control center 400. As shown in FIG. 4, the **central** monitoring and control ...all of computer system 410 could be incorporated into an application-specific or general-use **integrated circuit** .

Optional video display 440 is any type of video display suitable for interacting with a...

...similar video display. As discussed further below in conjunction with FIGS. 5 and 6, the **central** monitoring and control center 400 performs ...Generally, the data collection process 500 coordinates the collection

of data from one or more **semiconductor** factories 200. The preventative maintenance learning process 600 analyzes data that is 5 collected from equipment in a **semiconductor** factory following a failure using pattern recognition techniques to identify patterns in the data that...format. Alternatively, the network interface cards 230 can just forward the raw data to the **central** monitoring and control center 400 for translation and further processing. In addition, the extraction of relationship information may be performed by either the distributed network interface cards 230 or the **central** monitoring and control center 400.

As shown in FIG. 5, the exemplary data collection process...the present invention. As previously indicated, the 'data that is collected from equipment in a **semiconductor** factory is analyzed by the preventative maintenance learning process 600 following a failure using pattern... exemplary air composition monitor 700 shown in FIG. 7 monitors the air quality in a **semiconductor** factory 200 for a broad range of chemicals, for example, that may be harniful to...number of air hoses 720-1 through 720-N that may be distributed throughout a **semiconductor** factory 200. Generally, an interferometer in the air composition monitor 700 modulates a beam of...enables the remote configuration, operation and monitoring of the air composition monitor 700 in a **semiconductor** factory, as well as ...composition monitor 700 can accommodate the monitoring of new tools or new chemicals in the **semiconductor** factory 200. Specifically, new equipment 3 1 0 can be deployed with the functionality of...include XML, GIF/JPEG images, Java applets, or VBSCRIPT applets.

Typical standard reports in the **semiconductor** fabrication industly include materials consumption, waste production, yield parameter trends by equipment, standard yield parameter...of proprietary data or potential trade secret data can be put in place.

In a **semiconductor** application, users first select lots and wafers of interest and pick a report that is...index database (not shown), containing a list of all lots and wafers managed by the **central** monitoring and control center 400. When the user interacts with the data selector screen, the user is interfacing with CGI program and navigating the index **database** to select the lots and **wafers** of interest.

The data selector screen launches a separate web browser window to display reports...may be accessed even when contained within external databases. For example, if one was manufacturing **semiconductor** devices and needed to look at the 1 5 contact resistance, one may also be... storage systems. The network interface cards 230 of the present invention can be coupled to **databases** or other like memory **storage** locations. In this embodiment, the network interface cards 230 read the raw data to create...interface as one WO 03/040882 PCT/US02/35415 format files within a conventional file **storage** system outside of a **database** , where only the location and relationship of that data is maintained within the relational database...card 230 or optional server 240 serves to collect the raw data from programmable logic **controllers** 220 while maintaining relationships with the raw data. The present invention provides a portal ...can be extended beyond a single factory to many diverse applications, such as in the **semiconductor** industry where individual processes are outsourced to foundry or specialty operations, or where geographically diverse...

...printout of the data associated with that operation is returned with the product. Similarly, a **semiconductor** device completed ...a variety of diverse equipment systems is obtained via network connections. Processing may be either **centralized** at a network server or distributed to individual network interface cards 230 dependent on usage or function. When a **centralized** server processes data, processing requirements at the local level are minimized.

As long as the various equipment systems are capable of establishing a network connection, then the **centralized** server may process the data.

Additionally, this architecture minimizes the system requirements for the user...from any place in the world. This is particularly valuable for disperse manufacturing systems where **semiconductors** may be produced at a foundry in a country such as Taiwan and assembled in...materials are consumed. In this way, the manufacturing facility can achieve a Just-In-Time **inventory management system** for all consumable materials within ...reduced and the potential for aged raw materials is reduced.

The present invention allows the **semiconductor** factory 200 to optimize their chosen supply inventory. By tracking integrated data sets, one can ...1 0 are easily monitored by the present invention as they are added to a **semiconductor** factory 200, thus providing a scaleable solution.

It is to be understood that the embodiments...

Claim

1 . A method for remotely monitoring at least one equipment device in a **semiconductor** factory, said method comprising:
providing an interface to said equipment device having at least two...is monitored in real time to automatically adjust one or more process parameters in said **semiconductor** factory.

11 The method of claim 1, wherein said data from said equipment device is ...

...device is monitored in real time to automatically detect completion of a task in said **semiconductor** factory.

14 The method of claim 1, wherein data from a plurality of equipment devices...

...predefined threshold.

15 A method for remotely monitoring at least one equipment device in a **semiconductor** factory, said method comprising:
collecting historical data regarding the operation of said equipment device;
detecting...device into a desired uniform format.

22 A method for analyzing a failure in a **semiconductor** factory, said method
comprising:
collecting historical data regarding the operation of a plurality of interrelated equipment devices that operate in said **semiconductor** factory;
detecting at least one failure in said **semiconductor** factory; and
analyzing said historical data for each of said plurality of interrelated equipment devices...uniform format.

24 A system for remotely monitoring at least one equipment device in a **semiconductor** factory, said system comprising:
a memory that stores computer-readable code; and
a processor operatively...is monitored in real time to automatically adjust one or more process parameters in said **semiconductor** factory.
1 5

34 The system of claim 24, wherein said data from said equipment...device is monitored in real time to automatically detect completion of a task in said **semiconductor** factory.

37 The system of claim 24, wherein data from a plurality of equipment devices...

...predefined threshold.

38 A system for remotely monitoring at least one equipment device in a

semiconductor factory, said system comprising:
a ...device into a desired uniform format.

45 A system for analyzing a failure in a **semiconductor** factory, said system
comprising:
a memory that stores computer-readable code; and
a processor operatively...data regarding the operation of a plurality of interrelated
equipment devices that operate in said **semiconductor** factory;
detect at least one failure in said **semiconductor** factory; and
analyze said historical data for each of said plurality of interrelated equipment devices...

13/3,K/17 (Item 11 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00372416 **Image available**
WAFER **DEFECT** MANAGEMENT SYSTEM
SYSTEME DE GESTION DES DEFAUTS DE PLAQUETTES
Patent Applicant/Assignee:
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Inventor(s):
LA Tho Le,
SHIAU Ying,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9713158 A1 19970410
Application: WO 96US13929 19960830 (PCT/WO US9613929)
Priority Application: US 95539913 19951006
Designated States: JP KR AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE
Publication Language: English
Fulltext Word Count: 4151

WAFER **DEFECT** MANAGEMENT SYSTEM
Fulltext Availability:
Detailed Description
Claims
English Abstract
An automated **wafer** defect **management system** in which **wafer** defect data are collected from wafer inspection instruments, converted into a standard data format and made available through a **central** database system to workstations for review, analysis, and evaluation.

French Abstract
...plaquettes, converties en format de donnees standard et, par un systeme de base de donnees **central** , mises a disposition des stations de travail en vue de revision, d'analyse et d...

Detailed Description
... mANAaDff= SYSTEM
BACKGROUND OF = INVENTION
lo Field of the Invention
This invention relates generally to **semiconductor** wafer manufacturing, and, more particularly, to an automated **semiconductor wafer** defect **management system** for productivity and yield improvement.

2* Discussion of the Related Art
Growing technological requirements and...

...quickly as possible and as close to real time as possible.

The character of the **semiconductor** industry is such that competition requires that products are

-designed,,. manufactured,, and marketed in the...

...fabrication technology keep pace with
the rapid improvements in the electronics industry.
As advances in **semiconductor** waf er manuf acturing
technology lead to more sophisticated instruments with
improved imaging and analysis...

...produces information not easily accessible to the
production process engineering community, In a well
equipped **semiconductor** wafer manufacturing fab,
analytical instruments produce data faster than can be
manually analyzed by engineers.

Making **semiconductor** wafer defect and
contamination data available on a timely basis
throughout the corporate engineering community...THE INVENTION
According to the present invention, the foregoing
advantages are attained by an automated **wafer** defect
management system in which **wafer** defect data are
collected from wafer inspection instruments, converted
into a standard data format, and transferred to a
central database system,
In accordance With another aspect of the invention
userinterface workstations are provided such...
...perform detailed analysis of
the wafer defect data and return the analyzed data to
the **central** database system. The data analysis
stations include the capability for defect
classification, image capture, surface...

...of the invention. In
the drawings.

Figure 1A shows a first embodiment of the
automated **wafer** defect **management system** of the present
invention.

Figure 1B shows a second embodiment of the
automated **wafer** defect **management system** of the present
invention.

Figure 2 shows an embodiment of the automated
wafer defect **management system** showing representative
components in accordance with the present invention.

Figure 3 shows selected display attributes...the present invention is
illustrated in Figure 1A. In'this embodiment there is
shown a **wafer** defect **management system** 20. In this
embodiment there is shown wafer inspection instrument
(WII 11) 22, wafer inspection...

...INSPEX, Inc,, Billerica, MA,
Referring now to Figure 2 there is shown a
representative defect **wafer management system** 65
utilizing the teaching of the present invention and is
considered by the inventors as...

...As can
be appreciated other equivalent servers could be used
as well as other equivalent **database** software programs.

Disk **storage** 82 consists of ten gigabytes and provides
data record ...connected
to Ethernet 66 and a microscope & stage unit 116
connected to a bitmap stage **controller** 118 which is
connected to Ethernet 66. Analysis lab 72 also shows

PC workstations 120...
...of an Ethernet 66 connection.

The operation of representative system 68 is as follows. The **central** database system installed on server so acquires information in real time from every inspection and and the **central** database. Off-loading the graphical processing from the server onto the respective workstation provides for...

Claim
le An automated **wafer** defect **data** **management** **system** , comprising:
at least one **wafer** inspection instrument;
means for collecting wafer defect data from said at least one **wafer** inspection instrument;
a **central** **database** system; and
means for storing **wafer** defect data in said **central** **database** system,

2 The system as in claim 1. further comprising means for converting collected wafer...

...further comprising:
at least one user interface workstation; and
means for transferring user selected converted **wafer** defect data from said **central** **database** system to said at least one user interface workstation,
4e The system as in Claim 3, wherein said **central** database system comprises:
a server;
a relational database installed on said server for organizing said...

...defect
data at said at least one data analysis station; and
means for transferring analyzed **wafer** defect data to said **central** **database** system.
1 5
7o The system as in Claim 6. further comprising means for converting...

...9, wherein said means
for creating said statistical and graphical representations is independent of said **central** database system.

11 The system as in Claim 10, wherein said means for creating said...process monitor and equipment monitor database.

16 The system as in Claim 15, wherein said **central** database system further comprises means for correlating said user selected analyzed data with said electrical...

13/3,K/18 (Item 12 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00365171 **Image available**
METHOD AND APPARATUS FOR AUTOMATED WAFER LEVEL TESTING AND RELIABILITY DATA ANALYSIS
PROCEDE ET DISPOSITIF SERVANT A CONTROLER AUTOMATIQUEMENT L'ETAT DE TRANCHES DE CIRCUITS INTEGRES ET A ANALYSER LES DONNEES DE FIABILITE
Patent Applicant/Assignee:

ADVANCED MICRO DEVICES INC,
Inventor(s):
TSIANG Jerry,
LANTZ Mikkel,
PENG Yeng-Kaung,
SHIAU Ying,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9705497 A1 19970213
Application: WO 96US12533 19960731 (PCT/WO US9612533)
Priority Application: US 95509362 19950731
Designated States: JP KR AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE
Publication Language: English
Fulltext Word Count: 4313

Fulltext Availability:
Detailed Description
Claims

English Abstract
Methods and apparatus are disclosed for testing **integrated circuits** at the wafer level and for integrating test results, calculation of lifetimes and generation of trend charts in a common **data base** following testing. A **wafer** tester **controller** is supplemented with additional hardware and software to avoid data transfer errors and facilitate processing and **storage** of test results. The **data base** is available over a network to all areas of an organization.

Detailed Description
... integrated
't labrication and more particularly to the f 'eld of
cl.-

aul
o
tescling **integrated circuits** fabricated on a **semiconductor** wailer, prior to dicing of the wafer.
Backaround Art
in the prior art, **semiconductor** devices such as **integrated circuits** , are fabricated starting with the wafer of crystalline silicon. The purity of the wafer is highs Components of an **integrated circuit** , such as resistors, transistors, diodes, et cetera are formed by selectively introducing impurities into portions...

...surface of the wafer. A multiple layer device is thus created. The multiple layers include **semiconductor** layers, insulating layers and conductive layers linking the various regions of the components of the **integrated circuit** device.

complex devices can be created by carefully defining the regions which are exposed to...

...to replicate the set of masks needed for fabriqat.4on of a particular device or **integrated circuit** so that many **integrated circuits** can be formed simultaneously on a single wafer, Figure la shows such a wafer. of...
...155
io controlled by a positioning mechanism 150 which operates under control. of a tester **controller** mounted within the cabinet of the wafer tester. The tester **controller** incorv=ates a comzuter with an input device, such as keyboard 140, disc drives 130, and a visual display 120.

-1 C; The tester **controller** is loaded with sof tware such as operating system 200 and tester control application

software...

...reach of
positioning arm 150 and its probe. Each wafer 170 contains a plurality of **semiconductor** devices, such as intearated circuits, each of which is to be tested. The tester **controller** seauences the test probe through the posJ6. I.:.-Ions needed to make a test on each **integrated circuit** on the wafer. This may be done by taking one measurement from each of the **integrated circuits** on the wafer before progressing to a second measurement to be taken from each of the **integrated circuits** on the wafer 2
or, alternatively, all measurements for an **integrated circuit** can he taken at one time bef ore moving an to the next **integrated circuit** of the wafer.

In the prior art, data captured by wafer tester 100 was extracted...

...and certain
calculations z;erformed, including calculation of an estimate of the lifetime of the **integrated circuit** associated with the set of measurements. The results of -the analysis, -Lncludi.ng the expected life time of an **integrated circuit** were entered into a data base which could be wideliv accessed throuchout the oraanization.

The...

...the prior art had several
def."c"iencies. First, test results from the tester is **controller** were printed and manual calculations were performed. Alternatively,, test results were manually entered into a...
...calculated by the
computer. Next the test results and calculation results were transferred to a **central** database. This increased the chance for error ~~in data transf A. I.~~ .

Another problem with...

...tester
with exnanded functionality and by providing a network connection between one or more tester **controllers** and an organizational data base.

Accordingly, one advantage of the invention resides in the ability...

...system having a
network, a wafer tester with an automatic test probe and a tester **controller** connected to a network and a database connected to the network receiving test results from the wafer tester. The system includes analysis software on the tester **controller** for processin4 test results to derive a predicted lifetime for each **integrated circuit** on a waf er being tested. The results of the lif etime calculation are written...

...may be connected to the
network and each may monitor wafers containing different types of **integrated circuits** .

The invention is also directed to a method of automatically testing **integrated circuits** fabricated on a wafer using a wafer tester by probing selected points

on each **integrated circuit** of a wafer to measure one or more electrical values, storing the values with data identifying the **integrated circuit** and wafer at the wafer tester, processing the values to produce an estimate of lifetime for the **integrated circuit** at the wafer tester, and storing the estimate of lifetime together with the values at...

...of the prior art.

Figure .-a is a representation of a silicon wafer with certain **integrated circuits** fabricated thereon. Figure 2 is a representation of the software suite utiIJ.zed wit'26...network to which it is attached. Exammles of networks is suitable for handling communications between **wafer** testers and an organizational **data base** would include TCP/IP networks, token ring networks, and many other common digital or analog...

...part of the network line card resident on the mother board of the wafer tester **controller** .

Figure 5 is a flow chart of the processing of the data gathered by the...

...is directed to take test measurements at (510) and store the results in the tester **controller** (520). At 530, one or more loop tests are conducted, deDending on the order in...

...taken from each 7C on the wafer prior to taking a different test from each **IC** on the wafer. In an another alternatlve, all tests for one **IC** are taken before moving to the next **IC** . The particular loop tests implemented at ste-D 530 are those designed to implement the...

Claim

... system comprising:
a network;
a wafer tester, Comprising an automatic test probe and a tester **controller** , connected to the network;
a database connected to the network receiving test results from the wafer tester, and
analysis software an the tester **controller** for processing test results to derive a predicted lifetime for each **integrated circuit** on a wafer being tested.

2 The wafer testing system of claim 3. further comprising:
means for writing the results of a lifetime calculation to the **database** .
3* The **wafer** testing system of claim 1 further comprising:
a memory or diskette containing program commands for...

...a plurality of wafer testers connected to the network,
6 A method of automatically testing **integrated circuits** fabricated on a wafer using a wafer tester commrising:
probing selected points an each **integrated circuit** of a wafer to measure one or more electrical values;
staring the values with data identifying the **integrated circuit** and wafer at the wafer tester;

.processing the values to produce an estimate of lifetime for the **integrated circuit** at the wafer tester, and
storing the estimate of lifetime together with the values at...
?

```
?ds

Set     Items   Description
S1     393921   RETICLE? OR MASK? OR PHOTOMASK? OR WAFER? OR RETICULE?
S2    3895433   STOCK? OR STORAGE? OR STORE? ? OR STORING OR INVENTORY? OR
            INVENTORI? OR WAREHOUS? OR SUPPLY? OR SUPPLIE???
S3    2194243   SEMICONDUCTOR? OR INTEGRATED()CIRCUIT? OR IC OR ICS
S4    1155681   DATABASE? OR DATA()BASE? OR DB OR DBS OR DBMS OR MANAGEMEN-
            T()SYSTEM? OR DATABANK? OR DATA()BANK? ? OR DATAFILE? OR DATA-
            ()FILE? ? OR DATA()MANAG?
S5        268   S1 AND S2 AND S3 AND S4
S6       1563   S1(5N)S4
S7      36415   S2(5N)S4
S8         23   S6 AND S7 AND S3
S9         14   RD (unique items)
S10         9   S9 NOT PY>2000
S11         1   S5 AND CENTRAL? AND CONTROLLER?
S12         9   S5 AND CENTRAL?
S13         8   S12 NOT S10
S14         6   RD (unique items)
S15       250   S5 AND S3/DE,TI
S16         1   S15 AND RETICLE? AND STOCK?
?show files
File   8:Ei Compendex(R) 1970-2004/May W5
         (c) 2004 Elsevier Eng.  Info. Inc.
File  35:Dissertation Abs Online 1861-2004/May
         (c) 2004 ProQuest Info&Learning
File 103:Energy SciTec 1974-2004/May B2
         (c) 2004 Contains copyrighted material
File 202:Info. Sci. & Tech. Abs. 1966-2004/May 14
         (c) 2004 EBSCO Publishing
File  65:Inside Conferences 1993-2004/Jun W1
         (c) 2004 BLDSC all rts. reserv.
File   2:INSPEC 1969-2004/May W5
         (c) 2004 Institution of Electrical Engineers
File 233:Internet & Personal Comp. Abs. 1981-2003/Sep
         (c) 2003 EBSCO Pub.
File  94:JICST-EPlus 1985-2004/May W3
         (c)2004 Japan Science and Tech Corp(JST)
File 438:Library Lit. & Info. Science 1984-2004/Apr
         (c) 2004 The HW Wilson Co
File 111:TGG Natl.Newspaper Index(SM) 1979-2004/Jun 08
         (c) 2004 The Gale Group
File 603:Newspaper Abstracts 1984-1988
         (c)2001 ProQuest Info&Learning
File 483:Newspaper Abs Daily 1986-2004/Jun 07
         (c) 2004 ProQuest Info&Learning
File   6:NTIS 1964-2004/Jun W1
         (c) 2004 NTIS, Intl Cpyrght All Rights Res
File 144:Pascal 1973-2004/May W5
         (c) 2004 INIST/CNRS
File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec
         (c) 1998 Inst for Sci Info
File  34:SciSearch(R) Cited Ref Sci 1990-2004/May W5
         (c) 2004 Inst for Sci Info
File  62:SPIN(R) 1975-2004/Apr W3
         (c) 2004 American Institute of Physics
File  99:Wilson Appl. Sci & Tech Abs 1983-2004/Apr
         (c) 2004 The HW Wilson Co.
?
```

t's10/5/6,7,8

10/5/6 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

4562982 INSPEC Abstract Number: B9402-0170E-005, C9402-7160-005
Title: Integrating expert systems with a relational database in semiconductor **manufacturing**
Author(s): Perez, R.A.; Koh, S.W.
Author Affiliation: Dept. of Comput. Sci. & Eng., Univ. of South Florida, Tampa, FL, USA
Journal: IEEE Transactions on Semiconductor Manufacturing vol.6, no.3 p.199-206
Publication Date: Aug. 1993 Country of Publication: USA
CODEN: ITSMED ISSN: 0894-6507
U.S. Copyright Clearance Center Code: 0894-6507/93/$03.00
Language: English Document Type: Journal Paper (JP)
Treatment: Practical (P)
Abstract: The design and implementation of two expert systems for **semiconductor** manufacturing are described and compared. The first expert system is used for parametric test analysis in a CMOS wafer facility. It is designed as a user-interactive system, with all the expert's knowledge included in one knowledge base. This expert system tightly controls the flow of information between the knowledge base and the **wafer** data **stored** in a relational **database** . This expert system was implemented using the knowledge engineering environment shell with interface programs to INGRES. The second expert system is used for parametric test analysis in an analog wafer facility. This system is partitioned into several independent C programs running online and continuously communicating their results through the relational database. The interactive system is more flexible in representing expert knowledge and in explaining results, while the online system is faster, more open to new module integration, and better able to classify and diagnose large volumes of wafer data. (15 Refs)
Subfile: B C
Descriptors: CMOS **integrated circuits** ; expert systems; **integrated circuit** manufacture; linear **integrated circuits** ; manufacturing data processing; relational databases
Identifiers: expert systems; relational database; **semiconductor** manufacturing; parametric test analysis; CMOS wafer facility; user-interactive system; knowledge base; INGRES; analog wafer facility; C programs
Class Codes: B0170E (Production facilities and engineering); B2570 (Semiconductor integrated circuits); C7160 (Manufacturing and industry); C6170 (Expert systems); C6160D (Relational DBMS); C7480 (Production engineering)

10/5/7 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

03986609 INSPEC Abstract Number: B91063052, C91066079
Title: A modular expert system design for diagnosing semiconductor **wafers**
Author(s): Perez, R.A.; Sarmiento, C.D.; Victor, P.J.; Koh, S.W.
Author Affiliation: Dept. of Comput. Sci. & Eng., Univ. of South Florida, Tampa, FL, USA
Conference Title: Tenth International Workshop. Expert Systems and their Applications. Specialized Conference: Artificial Intelligence and Electrical Engineering p.153-64
Publisher: EC2, Nanterre, France
Publication Date: 1990 Country of Publication: France 352 pp.
ISBN: 2 906899 44 5
Conference Date: 28 May-1 June 1990 Conference Location: Avignon, France
Language: English Document Type: Conference Paper (PA)

Treatment: Practical (P)
Abstract: ADEPT is an expert system that was developed between the University of South Florida and Harris **Semiconductor** . This system examines **semiconductor** wafer parametric data from analog-type wafers, classifies the wafers, and determines the probable causes of failed wafers. This expert system interfaces with a relational **database** to retrieve the wafer parametric data from the **database** , and also to **store** the diagnostic results. The expert system is partitioned into several independent C programs running online and continuously communicating their individual results through the database. The system was buffered, modularized, and pipelined to keep up with the large amount of incoming data. The paper discusses the factors that influenced the choice of design as well as the most important features of the system. Conclusions based on the experiences during the design and implementation of this system in a computer integrated manufacturing environment are presented. (6 Refs)
Subfile: B C
Descriptors: analogue circuits; circuit analysis computing; expert systems; failure analysis; **integrated circuit** manufacture; **integrated circuit** testing; knowledge engineering; relational databases; VLSI
Identifiers: VLSI; modular expert system; **semiconductor** wafers; ADEPT; analog-type wafers; relational database; parametric data; computer integrated manufacturing
Class Codes: B2570 (Semiconductor integrated circuits); B0170E (Production facilities and engineering); B1130B (Computer-aided circuit analysis and design); C7410D (Electronic engineering); C6170 (Expert systems); C6160D (Relational DBMS)

10/5/8 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC

02032964 INSPEC Abstract Number: B83024225
Title: Reticle inspection technology to compare the pattern against data
Author(s): Awamura, D.
Author Affiliation: NJS Corp., Yokohama, Japan
Journal: Proceedings of the SPIE - The International Society for Optical Engineering vol.334 p.208-15
Publication Date: 1982 Country of Publication: USA
CODEN: PSISDG ISSN: 0277-786X
Conference Title: Optical Microlithography. Technology for the Mid-1980s
Conference Date: 31 March-1 April 1982 Conference Location: Santa Clara, CA, USA
Language: English Document Type: Conference Paper (PA); Journal Paper (JP)
Treatment: Practical (P)
Abstract: Describes a newly developed and very innovative reticle inspection system, the purpose of which is to make a comparison between the **reticle** pattern and the **data base stored** on the mag tape. Also includes the operational report from a couple of **semiconductor** companies where the systems are already installed and are operating very successfully. The system is capable of providing all the necessary information regarding the detected defects, such as location and type to the plotter, repair system (Zapper) and other peripherals by either on-line or off-line methods. One of the key features of this system is that all the defects detected electronically can be reviewed and confirmed by the human eye. The use of this system is expected to result in a higher device yield. (0 Refs)
Subfile: B
Descriptors: automatic testing; inspection; masks; **semiconductor** device manufacture
Identifiers: **semiconductor** device manufacture; reticle inspection system; reticle pattern; data base; mag tape; repair system; device yield
Class Codes: B0170L (Inspection and quality control); B2550 (Semiconductor device technology); B2550G (Lithography)
?

defect problems can be dramatically reduced.

English Descriptors: Tool management; Software; **Wafer** ; Learning; **Database** ; Information **storage** ; Review; Data analysis; Lithography; **Mask** ; Microelectronic fabrication

French Descriptors: Gestion outil; Logiciel; Pastille electronique; Apprentissage; Base donnee; **Stockage** information; Article synthese; Analyse donnee; Lithographie; Masque; Fabrication microelectronique

?t s14/5/1,2,3,4,5,6

14/5/1 (Item 1 from file: 8)

06707357 E.I. No: EIP04068006302

Title: Automated reticle **handling: A comparison of distributed and** centralized reticle storage **and transport**

Author: Murray, Anne M.; Miller, David J.
Corporate Source: Hudson Valley Research Park IBM Microelectronics M/S 56A, Hopewell Junction, NY 12603, United States

Conference Title: Proceedings of the 2003 Simulation Conference: Driving Innovation
Conference Location: New Orleans, LA, United States Conference Date: 20031207-20031210
Sponsor: ASA; ACM/SIGSIM; IEEE/CS; IEEE/SMC
E.I. Conference No.: 62143
Source: Winter Simulation Conference Proceedings v 2 2003. p 1360-1365 (IEEE cat n 03CH37499)
Publication Year: 2003
CODEN: WSCPDK ISSN: 0275-0708
Language: English
Document Type: CA; (Conference Article) Treatment: T; (Theoretical); X; (Experimental)
Journal Announcement: 0402W2

Abstract: The implementation of Automated Material Handling Systems (AMHS) in 300mm **semiconductor** facilities provides the opportunity to realize significant benefits in fabricator productivity and performance. The leverage associated with automated **reticle** delivery to photolithography process tools may be less apparent than a fab-wide AMHS. However, a high product mix environment requires the tracking, **storage** and transportation of thousands of **reticles** to successfully process **wafers** on photolithography tools. The failure to deliver **reticles** in an accurate and timely manner will negate many of the competitive advantages associated with automated **wafer** handling. Implementing an automated **reticle management system** (ARMS) requires an evolution from traditional **reticle storage** and management methodologies. In this paper, we review the application of simulation analysis to explore **centralized** versus distributed **reticle storage** and handling alternatives for an overall ARMS strategy. 7 Refs.

Descriptors: Materials handling; Freight transportation; Photolithography ; **Storage** (materials); Production; Product development; Statistical methods; Computer simulation
Identifiers: Automated **reticle** handling; Automated material handling systems (AMHS)
Classification Codes:
714.2 (Semiconductor Devices & Integrated Circuits); 694.4 (Storage); 913.1 (Production Engineering); 922.2 (Mathematical Statistics); 723.5 (Computer Applications)
691 (Bulk Handling & Unit Loads); 431 (Air Transportation); 714 (Electronic Components & Tubes); 694 (Packaging); 913 (Production Planning & Control; Manufacturing); 922 (Statistical Methods); 723 (Computer Software, Data Handling & Applications)
69 (MATERIALS HANDLING); 43 (TRANSPORTATION); 71 (ELECTRONICS & COMMUNICATION ENGINEERING); 91 (ENGINEERING MANAGEMENT); 92 (ENGINEERING MATHEMATICS); 72 (COMPUTERS & DATA PROCESSING)

14/5/2 (Item 2 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05967285 E.I. No: EIP01536782867
Title: Wafer **traveler design for an undergraduate microchip fabrication facility**
Author: Eckerman, P.D.; Hendricks, R.W.
Corporate Source: Mgmt. Sci. and Info. Technol. Dept. Virginia Polytech. Inst./State Univ., Blacksburg, VA 24016, United States
Conference Title: 14th Biennial University/Goverment/Industry Microelectronics Symposium
Conference Location: Richmond, VA, United States Conference Date: 20010617-20010620
Sponsor: IEEE; Virginia Economic Development Partnership; Greater Richmond Partnership
E.I. Conference No.: 58878
Source: Biennial University/Government/Industry Microelectronics Symposium - Proceedings 2001. p 120-124 (IEEE cat n 01CH37197)
Publication Year: 2001
ISSN: 0749-6877
Language: English
Document Type: CA; (Conference Article) Treatment: G; (General Review)
Journal Announcement: 0113W1
Abstract: In support of a new 1,800 ft**2 Class 10,000 cleanroom dedicated to teaching the elements of the microchip fabrication, we are developing a laboratory information **management system** (LIMS) that provides for the paperless operation of the facility. An essential part of this system is an electronic traveler that accompanies each **wafer** , tracking all changes and tests performed on it. This traveler replaces a student's lab notes and has the power of automatically recording all processing steps, accurately **storing** results of all tests performed, and being secured against unauthorized access. A custom-built Visual Basic application manages the flow of data from students to the **centralized database** . Both local and remote access to the **wafer** data is handled through a standard World Wide Web (WWW) browser. Students are allowed access to data only from **wafers** that they have been assigned to work on. As an added feature, the Microsoft Office suite of applications has been automated to assist students in the creation of charts and graphs that can be used to prepare lab reports and presentations. 3 Refs.
Descriptors: Information management; Laboratories; **Semiconductor** device manufacture; World Wide Web; Teaching
Identifiers: Microchip fabrication; Electronic traveler
Classification Codes:
903.2 (Information Dissemination); 714.2 (Semiconductor Devices & Integrated Circuits); 901.2 (Education)
903 (Information Science); 714 (Electronic Components & Tubes); 716 (Electronic Equipment, Radar, Radio & Television); 901 (Engineering Profession)
90 (ENGINEERING, GENERAL); 71 (ELECTRONICS & COMMUNICATION ENGINEERING)

14/5/3 (Item 3 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04320419 E.I. No: EIP95102906376
Title: Automation in semiconductor **production minienvironments, flexibility and information flow**
Author: Dudde, Ralf; Staudt-Fischbach, Peter; Herzog, Olaf
Corporate Source: Fraunhofer-Inst. for Silicon Technology, Itzehoe, Ger
Conference Title: Process, Equipment, and Materials Control in Integrated Circuit Manufacturing
Conference Location: Austin, TX, USA Conference Date: 19951025-19951026
Sponsor: SPIE - Int Soc for Opt Engineering, Bellingham, WA USA
E.I. Conference No.: 22403

· Source: Proceedings of SPIE - The International Society for Optical Engineering v 2637 1995. Society of Photo-Optical Instrumentation Engineers, Bellingham, WA, USA. p 158-167
Publication Year: 1995
CODEN: PSISDG ISSN: 0277-786X ISBN: 0-8194-2003-4
Language: English
Document Type: CA; (Conference Article) Treatment: M; (Management Aspects)
Journal Announcement: 9602W4
Abstract: The productivity of **semiconductor** fabs can be improved significantly by the combined action of several measures: Usage of expensive resources only at the point of use, like limiting the generation of a particlefree clean room environment to the immediate surrounding of **wafers** and **wafer** processed by usage of mini-environments and SMIF- **wafer** capsulation. Improvement of the logistic and material flow by an appropriate computer control system in the production line especially for a flexible **IC** - production. With its new Institute of Silicon Technology (ISiT) in Itzehoe the Fraunhofer-Society for applied research is now realizing an advanced CMOS pilot-line starting with a 0.5 mu process that is dedicated from the very beginning for an optimum in flexibility, productivity and lowest running costs. The complete concept for mini-environments, SMIF upgrade of the equipment and production control software was developed in a cooperation between the Fraunhofer institutes for Silicon Technology (ISiT) and Production automation (IPA). The Jenoptic, Jena, was chosen as **supplier** of SMIF components, mini-environments and identification software. The Line-Information- System, which operates as a low-cost manufacturing execution system, has been developed by the Fraunhofer-IPA using a **central database** system and client applications to access it. It tracks the actual work in progress in the fab, maintains equipment and lot history and allows production and cost monitoring and optimization. 5 Refs.
Descriptors: **Integrated circuit** manufacture; Automation; **Semiconductor** device manufacture; Clean rooms; Silicon **wafers** ; Control systems; Computer applications; Flexible manufacturing systems; CMOS **integrated circuits** ; Productivity
Identifiers: **Semiconductor** production minienvironments; Information flow; Computer control systems; Cost monitoring
Classification Codes:
913.4.1 (Flexible Manufacturing Systems)
714.2 (Semiconductor Devices & Integrated Circuits); 731.1 (Control Systems); 723.5 (Computer Applications); 913.4 (Manufacturing)
714 (Electronic Components); 731 (Automatic Control Principles); 723 (Computer Software); 913 (Production Planning & Control); 911 (Industrial Economics); 912 (Industrial Engineering & Management)
71 (ELECTRONICS & COMMUNICATIONS); 73 (CONTROL ENGINEERING); 72 (COMPUTERS & DATA PROCESSING); 91 (ENGINEERING MANAGEMENT)

14/5/4 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

4540251 INSPEC Abstract Number: B9401-0170E-022, C9401-7480-094
Title: Supporting semiconductor **manufacturing simulation tools using a structured data model**
Author(s): Baum, S.S.; Glassey, P.G.
Author Affiliation: NCR Microelectronic Products, Fort Collins, CO, USA
Conference Title: 1992 Winter Simulation Conference Proceedings (Cat. No.92CH3202-9) p.879-84
Publisher: IEEE, New York, NY, USA
Publication Date: 1992 Country of Publication: USA xxx+1410 pp.
ISBN: 0 7803 0798 4
Conference Sponsor: IEEE; ASA; ACM; IIE; NIST; ORSA; TIMS; SCS
Conference Date: 13-16 Dec. 1992 Conference Location: Arlington, VA, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P)

Abstract: A structured data modeling approach which is used to maintain and support two different simulation tools is discussed. The data model is **stored** in a relational **database** system which provides the links for each tool to access the data. One tool provides short interval production schedules for **semiconductor** manufacturing operations, and the other performs a wide variety of factory analyses on the same **wafer** fabrication plants. User interfaces were built on this system; they enable end users to run simulations of both experimental and actual situations. The use of the data model in linking manufacturing users to simulation tools is reviewed, and the advantages and disadvantages of using multiple tools and a **central database** are discussed. (5 Refs)

Subfile: B C

Descriptors: computer aided production planning; data structures; digital simulation; electronic engineering computing; **integrated circuit** manufacture; relational **databases** ; scheduling; **semiconductor** device manufacture; user interfaces

Identifiers: user interfaces; **semiconductor** manufacturing simulation tools; structured data model; relational **database** system; short interval production schedules; factory analyses; **wafer** fabrication plants

Class Codes: B0170E (Production facilities and engineering); B2560 (Semiconductor devices); B2570 (Semiconductor integrated circuits); B0170G (General fabrication techniques); C7480 (Production engineering); C7410D (Electronic engineering); C6160D (Relational DBMS); C6120 (File organisation)

14/5/5 (Item 2 from file: 2)

02636486 INSPEC Abstract Number: B86021746, C86020392

Title: Total evaluation system for VLSI process (systematized evaluation system)

Author(s): Kotani, N.; Yamano, T.; Kawazu, S.

Author Affiliation: LSI Res. & Dev. Lab., Mitsubishi Electr. Corp., Itami, Hyogo, Japan

Conference Title: 1985 International Symposium on VLSI Technology, Systems and Applications. Proceedings of Technical Papers p.63-7

Publisher: ERSO, Hsinchu, Taiwan

Publication Date: 1985 Country of Publication: Taiwan 355 pp.

Conference Sponsor: Nat. Sci. Council; Ind. Technol. Res. Inst

Conference Date: 8-10 May 1985 Conference Location: Taipei, Taiwan

Language: English Document Type: Conference Paper (PA)

Treatment: Practical (P)

Abstract: A total evaluation system for VLSI **wafer** process is established. Process parameters, inspection results, DC parametric test results and functional test results are gathered by subsystems and are transferred to **central** system. A **database** is used for data **storage** and data retrieving/processing is performed by a general purpose software system. Many kinds of information can be obtained by combining the **stored** data utilizing the powerful data processing capability. The required data for the process evaluation are provided in the forms of charts and tables. Thus, engineers can apply immediately the results to the process improvements. It has been found that this system is a powerful tool for the VLSI development and manufacturing. (2 Refs)

Subfile: B C

Descriptors: **database management systems** ; electronic engineering computing; **integrated circuit** manufacture; **integrated circuit** testing; manufacturing data processing; VLSI

Identifiers: **IC** technology; **DBMS** ; total evaluation system; VLSI **wafer** process; inspection results; DC parametric test results; functional test results; **database** ; manufacturing

Class Codes: B0170E (Production facilities and engineering); B2570 (Semiconductor integrated circuits); C7410D (Electronic engineering)

14/5/6 (Item 1 from file: 144)

16362884 PASCAL No.: 03-0529677

Yield Mask : **(The first professional Yield Management tool specifically developed for a** Mask **house)**

19th European conference on mask **technology for** integrated circuits **and microcomponents : Sonthofen, 13-15 January 2003**

LAUBMEIER Rudolf; MACKENZIE Annemarie; STOCKMANN Gerd; SHAIK Sana; WHITE Steve

BEHRINGER Uwe FW, ed

Infineon Technologies, Mask House, Balanstrasse, 73, 81541 Munich, Germany; Electroglas Inc., 6024 Silver Creek Valley Road, San Jose, CA, United States

International Society for Optical Engineering, Bellingham WA, United States

European conference on mask technology for integrated circuits and microcomponents, 19 (Sonthofen DEU) 2003-01-13

Journal: SPIE proceedings series, 2003, 5148 200-209

ISBN: 0-8194-5018-9 ISSN: 1017-2653 Availability: INIST-21760; 354000117718710230

No. of Refs.: 1 ref.

Document Type: P (Serial); C (Conference Proceedings) ; A (Analytic)

Country of Publication: United States

Language: English

To support the continuing Defect Engineering activities in the Infineon **Mask** House, a professional analysis tool has been developed for Defect Yield Management, in collaboration with EGsoft. EGSoft is the software division of Electroglas Inc. and **suppliers** of the YieldManager < SUP T SUP M > product, used for Yield Management in numerous **wafer** fabs. The requirement for such a tool was catalysed by the ever-increasing demand for sophisticated defect analysis, to accelerate defect learning and the identification of major and minor defect-related-yield detractors. Yield **Mask** consists of a **database** , which **centrally stores** all relevant information from Defect Inspection, Repair and Review tools in the Infineon **Mask** House and an analysis tool, which allows users to analyse the data collected on their PC. The analysis tool can be divided into six major modules: Data Set Builder, **Mask** Map, Map Gallery, Image Gallery, Charting and Customise: The functionality of the above-mentioned modules is presented and their application in the analysis of defect data demonstrated. The tool is shown to be an invaluable, cost-effective labour-saving device in a high-end **Mask** House, where the time required to analyse and resolve defect problems can be dramatically reduced.

English Descriptors: Tool management; Software; **Wafer** ; Learning; **Database** ; Information **storage** ; Review; Data analysis; Lithography; **Mask** ; Microelectronic fabrication

French Descriptors: Gestion outil; Logiciel; Pastille electronique; Apprentissage; Base donnee; **Stockage** information; Article synthese; Analyse donnee; Lithographie; Masque; Fabrication microelectronique

Classification Codes: 001D03F17

?

?t s16/5/1

16/5/1 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05880491 E.I. No: EIP01356631842
Title: Automated reticle **delivery in a 300 mm fab**
Author: Johnson, C.
Corporate Source: PRI Automation, Billerica, MA, United States
Source: Semiconductor International v 24 n 6 June 2001. p 99-106
Publication Year: 2001
CODEN: SITLDD ISSN: 0163-3767
Language: English
Document Type: JA; (Journal Article) Treatment: T; (Theoretical)
Journal Announcement: 0109W1
Abstract: The requirements for **reticle** automation and the use of automated material handling systems (AMHS) for increasing the productivity are explored. **Reticle stockers** for accessing and controlling the **inventory** provides automatic ID tracking and secure **storage** area. Automated guided vehicles (AGV) and overhead transport (OHT) vehicles are the available delivery systems for the **reticles** having features like automation-compatible load ports, ability to communicate with the automation system and set of commands to move the **reticles** . **Reticle** management can be accomplished by the integration of software systems which include scheduling system, manufacturing execution system (MES), **reticle management system** (RMS) and material control system (MCS). (Edited abstract) 4 Refs.
Descriptors: **Semiconductor** device manufacture; Automation; Lithography; Materials handling; **Inventory** control; Computer software; Process control ; Intelligent control; Intelligent vehicle highway systems; Cost effectiveness
Identifiers: Automated material handling systems (AMHS); Automatic guided vehicles (AGV)
Classification Codes:
723.4.1 (Expert Systems)
714.2 (Semiconductor Devices & Integrated Circuits); 911.3 (Inventory Control); 723.4 (Artificial Intelligence); 731.1 (Control Systems); 406.1 (Highway Systems); 723.5 (Computer Applications); 911.2 (Industrial Economics)
714 (Electronic Components & Tubes); 731 (Automatic Control Principles & Applications); 691 (Bulk Handling & Unit Loads); 911 (Cost & Value Engineering; Industrial Economics); 723 (Computer Software, Data Handling & Applications); 406 (Highway Engineering)
71 (ELECTRONICS & COMMUNICATION ENGINEERING); 73 (CONTROL ENGINEERING); 69 (MATERIALS HANDLING); 91 (ENGINEERING MANAGEMENT); 72 (COMPUTERS & DATA PROCESSING); 40 (CIVIL ENGINEERING, GENERAL)
?

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?ds
Set     Items   Description
S1     393997   RETICLE? OR MASK? OR PHOTOMASK? OR WAFER? OR RETICULE?
S2    3381654   STOCK? OR STORAGE? OR INVENTORY? OR INVENTORI? OR WAREHOUS?
              OR SUPPLY? OR SUPPLIE???
S3    2194530   SEMICONDUCTOR? OR INTEGRATED()CIRCUIT? OR IC OR ICS
S4    1155904   DATABASE? OR DATA()BASE? OR DB OR DBS OR DBMS OR MANAGEMEN-
             T()SYSTEM? OR DATABANK? OR DATA()BANK? ? OR DATAFILE? ? OR DA-
             TA()FILE? ? OR DATA()MANAG?
S5         14   S1(10N)S2(10N)S3(10N)S4
S6          8   RD (unique items)
S7        209   S1 AND S2 AND S3 AND S4
S8        195   S7 AND S3/DE,TI
S9          5   S8 AND CENTRAL?
S10       137   S8 NOT PY>2000
S11       102   RD (unique items)
S12        13   S11 AND S1(5N)S4
S13        10   S12 NOT (S6 OR S9)
?show files
File   8:Ei Compendex(R) 1970-2004/May W5
         (c) 2004 Elsevier Eng.  Info. Inc.
File  35:Dissertation Abs Online 1861-2004/May
         (c) 2004 ProQuest Info&Learning
File 103:Energy SciTec 1974-2004/May B2
         (c) 2004 Contains copyrighted material
File 202:Info. Sci. & Tech. Abs. 1966-2004/May 14
         (c) 2004 EBSCO Publishing
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         (c) 2004 BLDSC all rts. reserv.
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         (c) 2004 Institution of Electrical Engineers
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         (c) 2003 EBSCO Pub.
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         (c)2004 Japan Science and Tech Corp(JST)
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         (c) 2004 The HW Wilson Co
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         (c) 2004 The Gale Group
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         (c)2001 ProQuest Info&Learning
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         (c) 2004 NTIS, Intl Cpyrght All Rights Res
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         (c) 2004 INIST/CNRS
File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec
         (c) 1998 Inst for Sci Info
File  34:SciSearch(R) Cited Ref Sci 1990-2004/May W5
         (c) 2004 Inst for Sci Info
File  62:SPIN(R) 1975-2004/Apr W3
         (c) 2004 American Institute of Physics
File  99:Wilson Appl. Sci & Tech Abs 1983-2004/May
         (c) 2004 The HW Wilson Co.
?
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6/5/8 (Item 1 from file: 103)
DIALOG(R)File 103:Energy SciTec

00645659 ERA-05-027611; EDB-80-085184
Author(s): Doyal, L.A.; Weaver, D.L.; Gwyn, C.W.
Title: Computer control and data management in an LSI fabrication facility
Corporate Source: Sandia National Labs., Albuquerque, NM (USA)
Publication Date: Jun 1980
p 25
Report Number(s): SAND-80-0810
Contract Number (DOE): AC04-76DP00789
Document Type: Report
Language: English
Journal Announcement: EDB8007
Availability: NTIS, PC A02/MF A01.
Subfile: ERA (Energy Research Abstracts); TIC (Technical Information Center).
Country of Origin: United States
Country of Publication: United States
Abstract: A minicomputer system is used to control diffusion furnaces, monitor temperatures, provide operator instructions for each processing step, and record detailed process histories for **wafer** lots fabricated in the Sandia **Semiconductor** Development Laboratory. The system provides a complete **data base** for laboratory operations, a variety of displays describing equipment status, scheduling and utilization summaries for equipment, **wafer** and **mask inventories** , and laboratory management information. The **wafer** lot history includes a record indicating the operator, time, date, and specification recipe for each process step, special notes summarizing process deviations, results of inspection steps, and in-line capacitance, oxide thickness, or resistivity measurements.;
Major Descriptors: *INTEGRATED CIRCUITS -- FABRICATION
Descriptors: AUTOMATION; COMPUTERIZED CONTROL SYSTEMS; CONTROL SYSTEMS; MICROPROCESSORS; OPERATION; SEMICONDUCTOR DEVICES
Broader Terms: CONTROL SYSTEMS; ELECTRONIC CIRCUITS; MICROELECTRONIC CIRCUITS
Subject Categories: 420800* -- Engineering -- Electronic Circuits & Devices -- (-1989)
?

?t s9/5/2

9/5/2 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

5276076 INSPEC Abstract Number: B9607-2570D-012, C9607-7480-018
Title: Automation in semiconductor **-production minienvironments, flexibility and information-flow**
Author(s): Dudde, R.; Staudt-Fischbach, P.; Herzog, O.
Author Affiliation: Fraunhofer-Inst. for Silicon Technol., Itzehoe, Germany
Journal: Proceedings of the SPIE - The International Society for Optical Engineering Conference Title: Proc. SPIE - Int. Soc. Opt. Eng. (USA) vol.2637 p.158-67
Publisher: SPIE-Int. Soc. Opt. Eng,
Publication Date: 1995 Country of Publication: USA
CODEN: PSISDG ISSN: 0277-786X
SICI: 0277-786X(1995)2637L.158:ASPM;1-C
Material Identity Number: C574-95273
U.S. Copyright Clearance Center Code: 0 8194 2003 4/95/$6.00
Conference Title: Process, Equipment, and Materials Control in Integrated Circuit Manufacturing
Conference Sponsor: SPIE
Conference Date: 25-26 Oct. 1995 Conference Location: Austin, TX, USA
Language: English Document Type: Conference Paper (PA); Journal Paper (JP)
Treatment: Practical (P)
Abstract: The productivity of **semiconductor** fabs can be improved significantly by the combined action of several measures: usage of expensive resources only at the point of use, such as limiting the generation of a particle free clean room environment to the immediate surroundings of **wafers** and **wafer** processes by use of mini-environments and SMIF (standard mechanical interface) **wafer** encapsulation; also, improvement of the logistic and material flow by an appropriate computer control system in the production line especially for a flexible **IC** production. With its new Institute for Silicon Technology (ISiT) in Itzehoe, the Fraunhofer Society for applied research is now realizing an advanced CMOS pilot-line starting with a 0.5 mu m process dedicated to optimum flexibility and productivity with low running costs. The concept for mini-environments and SMIF upgraded equipment and production control software was developed in a cooperation between ISiT and the Fraunhofer Institute for Production Automation (IPA). Jenoptik of Jena was chosen as **supplier** of SMIF components, mini-environments and identification software. The line information system, which operates as a low-cost manufacturing execution system was developed by IPA using a **central database** system and client applications to access it. It tracks work in progress, maintains equipment and lot history and allows production and cost monitoring and optimization. (5 Refs)
Subfile: B C
Descriptors: clean rooms; CMOS **integrated circuits** ; computer integrated manufacturing; computerised monitoring; **database management systems** ; environmental engineering; flexible manufacturing systems; **integrated circuit** design; **integrated circuit** manufacture; manufacturing data processing; manufacturing resources planning; optimisation; process control; production control
Identifiers: automation; **semiconductor** -production minienvironments; Institute for Silicon Technology; information-flow; productivity; **semiconductor** fabs; particle free clean room environment; **wafers** ; **wafer** processes; mini-environments; SMIF **wafer** encapsulation; standard mechanical interface; material flow; computer control system; production line; flexible **IC** production; CMOS pilot-line; running costs; production control software; optimization; **central database** system; monitoring; 0.5 micron; Si
Class Codes: B2570D (CMOS integrated circuits); B0170E (Production facilities and engineering); B0170C (Project and design engineering); C7480 (Production engineering computing); C3355Z (Control applications in other

manufacturing processes); C3350E (Control applications in the electronics industry); C7410D (Electronic engineering computing); C7160 (Manufacturing and industrial administration); C6160 (Database management systems (DBMS)) ; C7410H (Computerised instrumentation)
Chemical Indexing:
Si int - Si el (Elements - 1)
Si sur - Si el (Elements - 1)
Numerical Indexing: size 5.0E-07 m

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?t s13/5/3,9

13/5/3 (Item 3 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05056758 E.I. No: EIP97093812163
Title: Real-time line-width measurements: a new feature for reticle inspection systems
Author: Eran, Yair; Greenberg, Gad; Joseph, Amnon; Lustig, Cornel; Mizrahi, Eyal
Corporate Source: Orbot Instruments Ltd., Yavne, Isr
Conference Title: Photomask and X-Ray Mask Technology IV
Conference Location: Kawasaki City, Jpn Conference Date: 19970417-19970418
Sponsor: SPIE - Int Soc for Opt Engineering, Bellingham, WA USA
E.I. Conference No.: 23036
Source: Proceedings of SPIE - The International Society for Optical Engineering v 3096 1997. Society of Photo-Optical Instrumentation Engineers, Bellingham, WA, USA. p 480-491
Publication Year: 1997
CODEN: PSISDG ISSN: 0277-786X ISBN: 0-8194-2516-8
Language: English
Document Type: CA; (Conference Article) Treatment: X; (Experimental); A ; (Applications)
Journal Announcement: 9809W1
Abstract: The significance of line width control in **mask** production has become greater with the lessening of defect size. There are two conventional methods used for controlling line widths dimensions which employed in the manufacturing of **masks** for sub micron devices. These two methods are the critical dimensions (CD) measurement and the detection of edge defects. Achieving reliable and accurate control of line width errors is one of the most challenging tasks in **mask** production. Neither of the two methods cited above (namely CD measurement and the detection of edge defects) guarantees the detection of line width errors with good sensitivity over the whole **mask** area. This stems from the fact that CD measurement provides only statistical data on the **mask** features whereas applying edge defect detection method checks defects on each edge by itself, and does not **supply** information on the combined result of error detection on two adjacent edges. For example, a combination of a small edge defect together with a CD non- uniformity which are both within the allowed tolerance, may yield a significant line width error, which will not be detected using the conventional methods (see figure 1). A new approach for the detection of line width errors which overcomes this difficulty is presented. Based on this approach, a new sensitive line width error detector was developed and added to Orbot's RT-8000 die-to- **database** **reticle** inspection system. This innovative detector operates continuously during the **mask** inspection process and scans (inspects) the entire area of the **reticle** for line width errors. The detection is based on a comparison of measured line width that are taken on both the design **database** and the scanned image of the **reticle** . In section 2, the motivation for developing this new detector is presented. The section covers an analysis of various defect types, which are difficult to detect using conventional edge detection methods or, alternatively, CD measurements. In section 3, the basic concept of the new approach is introduced together with a description of the new detector and its characteristics. In section 4, the calibration process that took place in order to achieve reliable and repeatable line width measurements is presented. The description of an experiments conducted in order to evaluate the sensitivity of the new detector is given in section 5, followed by a report of the results of this evaluation. The conclusions are presented in section 6. 4 Refs.
Descriptors: Inspection; **Semiconductor** device manufacture; Real time systems; **Masks** ; Defects; Design; **Database** systems; Distance measurement
Identifiers: Critical dimensions; **Reticle** defects
Classification Codes:
913.3.1 (Inspection)

913.3 (Quality Assurance & Control); 714.2 (Semiconductor Devices & Integrated Circuits); 722.4 (Digital Computers & Systems); 723.3 (Database Systems); 943.2 (Mechanical Variables Measurements)
913 (Production Planning & Control); 714 (Electronic Components); 722 (Computer Hardware); 723 (Computer Software); 943 (Mechanical & Miscellaneous Measuring Instruments)
91 (ENGINEERING MANAGEMENT); 71 (ELECTRONICS & COMMUNICATIONS); 72 (COMPUTERS & DATA PROCESSING); 94 (INSTRUMENTS & MEASUREMENT)

13/5/9 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

5774336 INSPEC Abstract Number: B9801-0170E-031
Title: Implementation of a test wafer inventory **tracking system to increase efficiency in monitor** wafer **usage**
Author(s): Popovich, S.B.; Chilton, S.R.; Kilgore, B.
Author Affiliation: Motorola Inc., Chandler, AZ, USA
Conference Title: 1997 IEEE/SEMI Advanced Semiconductor Manufacturing Conference and Workshop. Theme - The Quest for Semiconductor Manufacturing Excellence: Leading the Charge into the 21st Century. ASMC Proceedings (Cat. No.97CH36089) p.440-3
Publisher: IEEE, New York, NY, USA
Publication Date: 1997 Country of Publication: USA vi+460 pp.
ISBN: 0 7803 4050 7 Material Identity Number: XX97-02429
U.S. Copyright Clearance Center Code: 0 7803 4050 7/97/$10.00
Conference Title: 1997 IEEE/SEMI Advanced Semiconductor Manufacturing Conference and Workshop ASMC 97 Proceedings
Conference Sponsor: Semicond. Equipment & Mater. Int. (SEMI); IEEE; IEEE Electron Devices Soc.; IEEE Components, Packaging & Manuf. Technol. Soc
Conference Date: 10-12 Sept. 1997 Conference Location: Cambridge, MA, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P)
Abstract: The process of building **integrated circuits** requires that **semiconductor** manufacturers spend millions of dollars annually on the purchase of test **wafers** . These test **wafers** are used to qualify tools, monitor processes, and develop new process techniques. Reducing the number of test **wafers** brought into the manufacturing process is critical to overall cost containment and improved efficiency. Other considerations for reducing the number of test **wafers** include the amount of time spent tracking down misplaced material, the potential for contamination and tool downtime if the wrong used test **wafers** are processed in the wrong tool, lost manufacturing capacity due to excessive **storage** of test material, and downtime resulting from a lack of test **wafers** due to poor test **wafer** management. In an effort to reduce costs spent on test **wafers** , many companies use reclaim to polish off the top surface of the test **wafer** . This provides a clean **wafer** suitable for re-use at a much reduced cost. In many cases, however, **wafers** are sent out for reclaim before their full internal re-use potential is realized, offsetting some of the cost savings. This is most likely due to the complexity in identifying downgrading paths and controlling the **inventory** of generated used test **wafers** . Motorola MOS12 recognized a need for a system that would significantly reduce the amount of money spent on test **wafers** by optimizing internal re-use opportunities implementation of this system required manufacturing and engineering to work together to determine which flows could be safely re-used and where, without negative impact to manufacturing. A matrix was constructed identifying all potential re-use opportunities. This system automates the test **wafer** ordering process, and forces used material to be used whenever possible, maximizing test **wafer** re-use. This paper win outline the necessary requirements for the development and installation of an efficient, automatic test **wafer management system** . (2 Refs)
Subfile: B
Descriptors: **integrated circuit** manufacture; **integrated circuit** testing; **stock** control
Identifiers: test **wafer inventory** tracking system; **wafer** usage

monitoring; **integrated circuit** manufacture; **semiconductor** fab; cost; efficiency; Motorola MOS12; internal re-use optimization; automatic **management system** ; downgrading path; reclaim

Class Codes: B0170E (Production facilities and engineering)

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?ds

Set     Items   Description
S1     341741   RETICLE? OR MASK? OR PHOTOMASK? OR WAFER? OR RETICULE?
S2   12263293   STOCK? OR STORAGE? OR INVENTORY? OR INVENTORI? OR WAREHOUS?
              OR SUPPLY? OR SUPPLIE???
S3    1290022   SEMICONDUCTOR? OR INTEGRATED()CIRCUIT? OR IC OR ICS
S4    2899475   DATABASE? OR DATA()BASE? OR DB OR DBS OR DBMS OR MANAGEMEN-
             T()SYSTEM? OR DATABANK? OR DATA()BANK? ? OR DATAFILE? ? OR DA-
             TA()FILE? ? OR DATA()MANAG?
S5       1165   S1 (5N)S4
S6     145787   S2(5N)S4
S7         17   S5(S)S6(S)S3
S8          8   RD (unique items)
S9       1258   S1(S)S2(S)3(S)4
S10       169   S1(10N)S2(10N)S4(10N)S3
S11        99   RD (unique items)
S12        82   S11 NOT PY>2000
S13        33   S12 AND S3/DE,TI
S14       134   S9 AND CENTRAL?
S15        58   S9(S)CENTRAL?
S16        47   RD (unique items)
S17        30   S16 NOT PY>2000
S18         2   S17 AND S3/DE,TI
S19        14   S14 AND S3/DE,TI
S20        10   RD (unique items)
?show files
File 275:Gale Group Computer DB(TM) 1983-2004/Jun 08
         (c) 2004 The Gale Group
File 621:Gale Group New Prod.Annou.(R) 1985-2004/Jun 04
         (c) 2004 The Gale Group
File 636:Gale Group Newsletter DB(TM) 1987-2004/Jun 07
         (c) 2004 The Gale Group
File  16:Gale Group PROMT(R) 1990-2004/Jun 08
         (c) 2004 The Gale Group
File 160:Gale Group PROMT(R) 1972-1989
         (c) 1999 The Gale Group
File 148:Gale Group Trade & Industry DB 1976-2004/Jun 08
         (c)2004 The Gale Group
File 624:McGraw-Hill Publications 1985-2004/Jun 07
         (c) 2004 McGraw-Hill Co. Inc
File  15:ABI/Inform(R) 1971-2004/Jun 08
         (c) 2004 ProQuest Info&Learning
File 647:CMP  Computer Fulltext 1988-2004/May W5
         (c) 2004 CMP Media, LLC
File 674:Computer News Fulltext 1989-2004/May W5
         (c) 2004 IDG Communications
File 369:New Scientist 1994-2004/May W5
         (c) 2004 Reed Business Information Ltd.
File   9:Business & Industry(R) Jul/1994-2004/Jun 07
         (c) 2004  The Gale Group
File  13:BAMP 2004/May W3
         (c) 2004  The Gale Group
File 610:Business Wire 1999-2004/Jun 08
         (c) 2004 Business Wire.
File 810:Business Wire 1986-1999/Feb 28
         (c) 1999 Business Wire
File  47:Gale Group Magazine DB(TM) 1959-2004/Jun 03
         (c) 2004 The Gale group
?
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?t s8/3,k/2,4,5,6

8/3,K/2 (Item 2 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

01582319 SUPPLIER NUMBER: 13356352 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Wafer fab: happy days again? (wafer fabrication equipment industry)
Dunn, Peter
Electronic News (1991), v39, n1944, p12(1)
Jan 4, 1993
ISSN: 1061-6624 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 1011 LINE COUNT: 00077

... growth in the second half of the year, says Mitch Tyson, executive vice president. Many **IC** producers are renovating and upgrading older fabs, and PRI is providing **reticle stockers** and work-in-progress **management systems** that become necessary when many different designs go through a single facility.
PRI finds most...

8/3,K/4 (Item 2 from file: 621)
DIALOG(R)File 621:Gale Group New Prod.Annou.(R)

02212148 Supplier Number: 56905326 (USE FORMAT 7 FOR FULLTEXT)
PRI Automation Announces New Combination Reticle Stocker.
PR Newswire, p9143
Oct 26, 1999
Language: English Record Type: Fulltext
Document Type: Newswire; Trade
Word Count: 920

... MCS.
According to figures released by Dataquest for calendar year 1998, PRI is the leading **supplier** of automated **reticle management systems** with over 65% market share. PRI has been shipping **reticle management systems** since 1991 and has an installed base of over one hundred systems. The new Combination Reticle Stocker has been installed at several leading **semiconductor** manufacturers and PRI has orders for additional systems currently in production.
About PRI Automation
PRI...

8/3,K/5 (Item 3 from file: 621)
DIALOG(R)File 621:Gale Group New Prod.Annou.(R)

01850012 Supplier Number: 54403945 (USE FORMAT 7 FOR FULLTEXT)
Asyst Technologies to Acquire Progressive System Technologies, Inc.
Business Wire, p0367
April 19, 1999
Language: English Record Type: Fulltext
Document Type: Newswire; Trade
Word Count: 810

... the leading supplier of Standard Mechanical InterFace (SMIF) isolation and manufacturing automation solutions to the **semiconductor** industry, announced today that it has signed a letter of intent to acquire Progressive System Technologies, Inc. (PST) (Austin, Texas), a **supplier** of substrate **management systems** for open-cassette, SMIF-integrated **wafer** logistics and reticle automation. With the acquisition, Asyst enhances its position as a leading global...

8/3,K/6 (Item 1 from file: 636)
DIALOG(R)File 636:Gale Group Newsletter DB(TM)

02211958 Supplier Number: 44199499 (USE FORMAT 7 FOR FULLTEXT)

Robotic retrieval system uses Permastat PP

High Performance Plastics, pN/A
Nov, 1993
Language: English Record Type: Fulltext
Document Type: Newsletter; Trade
Word Count: 177

US firm Precision Robots Inc, of Billerica, Massachusetts, manufactures an automation **storage** and inventory **management system** for **reticle** boxes. **Reticles** are the master pattern of the circuitry that is exposed by a photolithographic process onto **semiconductor** chips. The system is used within the clean chip manufacturing environment, and therefore shelf supports...

?

?t s13/3,k/7,9,12,14,16,20,28,29

13/3,K/7 (Item 4 from file: 621)
DIALOG(R)File 621:Gale Group New Prod.Annou.(R)

02246710 Supplier Number: 57889349 (USE FORMAT 7 FOR FULLTEXT)
Asyst Technologies Introduces New Reticle Management System; Shrinking Geometries Create New Market for Reticle Manipulation and Protection Platforms.
Business Wire, p0482
Dec 1, 1999
Language: English Record Type: Fulltext
Document Type: Newswire; Trade
Word Count: 773

... of the SEMICON Japan 99, Asyst Technologies, Inc. (Nasdaq/NM:ASYT) today unveiled its new **Reticle Management System** (RMS) for use in **semiconductor** manufacturing. A platform for manipulating and protecting valuable **reticles** from particulate contamination and other potential sources of damage, the RMS is designed for use by **semiconductor** device manufacturers, **photomask suppliers** (**mask** houses) and original equipment manufacturers (OEMs).

In **semiconductor** manufacturing, the RMS can be used in the photolithography area to manipulate and identify **reticles** during the manufacturing process. **Mask** houses can use the RMS to manipulate **reticles** at the incoming inspection stage, while OEMs are able to use the RMS as an...
NAICS CODES: 333295 (**Semiconductor** Machinery Manufacturing)

13/3,K/9 (Item 6 from file: 621)
DIALOG(R)File 621:Gale Group New Prod.Annou.(R)

01675671 Supplier Number: 50161272 (USE FORMAT 7 FOR FULLTEXT)
New Productivity Enhancement Software and Engineering Services Offered to IC Makers at Pay-For-Results Pricing.
Business Wire, p07130401
July 13, 1998
Language: English Record Type: Fulltext
Article Type: Article
Document Type: Newswire; Trade
Word Count: 1042

New Productivity Enhancement Software and Engineering Services Offered to IC Makers at Pay-For-Results Pricing.
... chart that depicts frequency of use in the facility over the equipment's life cycle.

Reticle Management System

TEFEN's third new product, its **Reticle Management System** , is the first software tool to help **IC** makers cut costs by automating the complex task of allocating and dispatching **reticles** , the "original masters" of circuit patterns to be printed across the surface of **semiconductor wafers** . With a typical **wafer** fabrication facility **stocking** 2,000 to 4,000 **reticles** , some on racks in **storage** and some set up in lots online waiting to be loaded on lithography systems, operators...

13/3,K/12 (Item 9 from file: 621)
DIALOG(R)File 621:Gale Group New Prod.Annou.(R)

01241056 Supplier Number: 44365769 (USE FORMAT 7 FOR FULLTEXT)
ASYST ANNOUNCES NEW MINIENVIRONMENT PRODUCT LINE FEATURING ADVANCED ERGONOMICS

News Release, pN/A
Jan 18, 1994
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 563

... is
based upon the utilization of the SMIF ("Standard Mechanical InterFace") standard, consisting of sealed **wafer** cassette containers,
processing equipment enclosures, and related indexer and robotic transfer equipment. The company also...

...family of SMART-
Traveler products, including software and electronic display and communication devices, which enable **semiconductor** manufacturers to track **wafers** and reduce misprocessing during the production of **integrated circuits** .
About Asyst: Asyst Technologies, Inc. is headquartered in Milpitas, Calif., with facilities in Colorado, Europe and the Far East. Asyst products give **IC** manufacturers enhanced environmental control in the cleanroom through the use of Isolation Technology. The system integrates process tool enclosures, **wafer** carriers, an automated cassette transfer system and a paperless **management system** for WIP control. Asyst's common **stock** is traded on the NASDAQ National Market System under the trading symbol ASYT.
NAICS CODES: 333295 (**Semiconductor** Machinery Manufacturing)

13/3,K/14 (Item 1 from file: 636)
DIALOG(R)File 636:Gale Group Newsletter DB(TM)

02684740 Supplier Number: 45445077 (USE FORMAT 7 FOR FULLTEXT)
MATERIAL HANDLING UPDATE: PRI IS IN THE CHIPS
Manufacturing Automation, v4, n7, pN/A
April, 1995
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 521

(USE FORMAT 7 FOR FULLTEXT)
TEXT:
...OR. Under the terms of the agreement, PRI will design and install an integrated transportation, **storage** , and **management system** - -including monorails, **stockers** , and control subsystems--used for moving eight -inch silicon **wafers** through the front end of the **semiconductor** manufacturing process performed at the world-class facility, which will be the first eight -inch **wafer** fab built by IDT.
NAICS CODES: 334413 (**Semiconductor** and Related Device Manufacturing)

13/3,K/16 (Item 2 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)

06056102 Supplier Number: 54175330 (USE FORMAT 7 FOR FULLTEXT)
Replacing Paper with PDM.
BMS
Computer-Aided Engineering, v17, n8, p12(1)
August, 1998
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Academic Trade
Word Count: 689

(USE FORMAT 7 FOR FULLTEXT)

TEXT:
KLA-Tencor is a leading **supplier** of **wafer** inspection equipment for the **semiconductor** industry. In September 1996, the company began deployment of a product **data management** (PDM) system **supplied** by Sherpa Corp. Previously, KLA-Tencor's engineering documentation process was entirely paper-based.
NAICS CODES: 51121 (Software Publishers); 333295 (**Semiconductor** Machinery Manufacturing)

13/3,K/20 (Item 6 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)

04098604 Supplier Number: 45973323 (USE FORMAT 7 FOR FULLTEXT)
Asyst Names New Head for Automation
Thin Film/Diamond Technology News, pN/A
Dec 1, 1995
Language: English Record Type: Fulltext
Document Type: Newsletter; Trade
Word Count: 244

... since booked more than $32 million in orders for its interbay and intrabay automation and **reticle - management systems** from major **IC** manufacturers worldwide, such as Advanced Micro Devices; Philips Electronics NV; SGS-Thompson; Seimens; Taiwan **Semiconductor** Manufacturing Co.; and Windbond. Automation is becoming an integral part in advanced **IC** fabs, with the automation market expected to reach more than $500 million by 2000.

Thin Film/Diamond Technology **Stock** Index

This	Last Company	Symbol	Month	Month	Change
	Applied Materials	AMAT	41.375	46.750...	

NAICS CODES: 334413 (**Semiconductor** and Related Device Manufacturing)

13/3,K/28 (Item 1 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB

07906752 SUPPLIER NUMBER: 16985135 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Asyst unveils semiconductor **industry's first 300mm wafer handling solution and its plan to openly license the revolutionary technology.**
Business Wire, p6011109
June 1, 1995
LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT
WORD COUNT: 1236 LINE COUNT: 00111

Asyst unveils semiconductor **industry's first 300mm wafer handling solution and its plan to openly license the revolutionary...**

TEXT:
MILPITAS, Calif.--(BUSINESS WIRE)--June 1, 1995--Asyst Technologies, Inc. (NASDAQ:ASYT), a leading **supplier** of automated material **management systems** for the global **semiconductor** industry, today unveiled the industry's first 300mm **wafer** handling solution -- the Asyst Auto-Kinematic(TM) Cassette. Simultaneously, the company announced plans to openly...

DESCRIPTORS: **Semiconductor** industry...

13/3,K/29 (Item 2 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB

07742269 SUPPLIER NUMBER: 16600913 (USE FORMAT 7 OR 9 FOR FULL TEXT)

PRI Automation wins $10 million order from Integrated Device Technology; Leading factory automation supplier to maximize efficiency of new specialty semiconductor **fab.**

Business Wire, p03010216

March 1, 1995

LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT

WORD COUNT: 403 LINE COUNT: 00036

...**order from Integrated Device Technology; Leading factory automation supplier to maximize efficiency of new specialty** semiconductor **fab.**

PRI Automation is the leading U.S. **supplier** of factory automation systems used by semiconductor manufacturing companies to optimize **integrated circuit** manufacturing.

Under the terms of the agreement, PRI will design and install an integrated transportation, **storage** and **management system** -- including monorails, **stockers** and control subsystems -- to move eight-inch silicon **wafers** through the front-end of the **semiconductor** manufacturing process at the IDT facility. This world-class facility will be the first eight-inch **wafer** fab built by IDT.

The contract calls for a phased approach to installation of the...

DESCRIPTORS: **Semiconductor** industry...

... **Semiconductor** production equipment

?

?t s13/9/9

13/9/9 (Item 6 from file: 621)
DIALOG(R)File 621:Gale Group New Prod.Annou.(R)

01675671 Supplier Number: 50161272 (THIS IS THE FULLTEXT)
New Productivity Enhancement Software and Engineering Services Offered to IC Makers at Pay-For-Results Pricing.
Business Wire, p07130401
July 13, 1998
Language: English Record Type: Fulltext
Article Type: Article
Document Type: Newswire; Trade
Word Count: 1042
TEXT:
FOSTER CITY, Calif.--(BUSINESS WIRE)--July 13, 1998--

Spare Parts Inventory, Cost of Ownership and Reticle Management Software Packages Reduce Costs for Wafer Fabs Without Bottom-Line Risk During IC Industry Downturn

With the cost of doing business continuing to rise for semiconductor device makers, TEFEN USA has released three new productivity enhancement products designed to help reduce overall manufacturing costs with virtually no bottom-line risk.

Expanding its line of value-adding software products, the international industrial engineering firm specializing in software and consulting services that improve manufacturing productivity will begin offering its three newest products -- its Spare Parts Inventory Model (SPIM(TM)), Cost of Ownership (COO), and Reticle Management System (RMS) tools -- in the third quarter of this year.

TEFEN is offering the new software applications in combination with its consulting services through an innovative "success-based" pricing model that rewards TEFEN with a percentage of cost reductions realized by its customers.

All three products are available for Windows 95, 98 and NT platforms and run with Microsoft Access(R) database management software. An intuitive point-and-click graphical user interface on the software requires minimal training for new users.

"With the global semiconductor market in a downturn, IC (integrated circuit) manufacturers worldwide are focusing intently today on improving their operating efficiencies and reducing costs associated with their manufacturing process," said Haim Albalak, president of TEFEN USA.

"With our new software tools and our success-based pricing strategy, TEFEN can accommodate the needs of our customers with immediate and innovative solutions to reduce costs and cycle times within their facilities."

Spare Parts Inventory Model

In any manufacturing industry and particularly in fast-paced business segments, such as semiconductor production, the rising costs of spare parts is driving the need to minimize inefficiencies through "just in time" inventory management.

TEFEN's new SPIM spare parts inventory modeling software assures this just-in-time process by automating the functions required to build an inventory management system, including usage, delivery times, costs, demands by various equipment, and quantities in stock.

As a result, warehouses decrease the overall cost of inventory by maintaining appropriate stock levels and reducing the workload on the purchasing department.

Unlike manual or less sophisticated inventory control methods, SPIM provides purchasing departments with a monthly planning tool that quickly and easily estimates future demand for spare parts.

Using linear regression modeling that predicts demand by charting historical use and fixing a linear view through those data points toward data points that represent future use, SPIM allows a facility to maintain optimal inventory levels of spare parts.

SPIM is designed to integrate into the overall dispatching system of a manufacturing facility and generates decision-critical reports that

identify obsolete inventory, maximum and minimum inventory levels, reorder points, and expected shipments.

Cost of Ownership Model

For businesses that are looking deeper for ways to cut costs, TEFEN's new cost of ownership software tool COO 1.0, allow them to identify potential cost savings in deciding which equipment to purchase and how to best use it within a production facility.

Manufacturing companies are increasingly aware that operating costs, incurred after the purchase date, often are greater than the price tag on a piece of capital equipment. TEFEN's COO 1.0 model gives decision makers a tool for extrapolating total costs into the future, whereas other cost of ownership tools do not.

Combining basic accounting principles and sophisticated engineering methodologies, such as staffing and tool/line capacity analyses, TEFEN's COO program assists manufacturers in comparing products prior to a purchasing decision, basing that comparison on the many factors that make up the real cost of a product over its lifetime.

Some of these factors might include all of a product's features, price, benefits, financing alternatives, equipment performance in terms of yield and throughput, direct and indirect labor costs, maintenance in terms of technicians' hours, spare parts and downtime, space requirements and utility needs. COO 1.0 breaks out the numbers in each of these categories and, for each product, generates investment and cost structure reports as well as a performance chart that depicts frequency of use in the facility over the equipment's life cycle.

Reticle Management System

TEFEN's third new product, its **Reticle Management System** , is the first software tool to help **IC** makers cut costs by automating the complex task of allocating and dispatching **reticles** , the "original masters" of circuit patterns to be printed across the surface of **semiconductor wafers** . With a typical **wafer** fabrication facility **stocking** 2,000 to 4,000 **reticles** , some on racks in **storage** and some set up in lots online waiting to be loaded on lithography systems, operators must which reticle lots are available, which are waiting and, more importantly, if those on the production line are the appropriate lots for the current work in progress.

TEFEN's reticle management software is a decision-support tool for the lithography system operator on the wafer fabrication line. It uses a "look ahead" approach to predict which lots are coming into their equipment and which are needed. This "look ahead" data is downloaded into the backbone of the system, the linear program module, which runs at the beginning of every shift and allocates the optimal ratio of reticles to steppers. The linear programming module then presents to the operator a computerized list of instructions for each reticle transaction in priority order.

"Simply stated, our Reticle Management System puts the right reticle at the right machine at the right time to maximize the yield of expensive lithography systems, produce fewer errors, and reduce the overall cost of owning and operating a semiconductor lithography system," said TEFEN's Albalak.

TEFEN is an international leader in industrial engineering and systems analysis. Founded in 1982, the company has amassed a worldwide reputation for success in improving and enhancing the production process of numerous semiconductor and electronics manufacturers. TEFEN's expertise included modeling facility layout and continuous productivity improvement. The company's client list includes some of the world's largest and fastest growing high-tech manufacturers. TEFEN maintains offices in the U.S., Europe, Israel, and Taiwan. TEFEN USA headquarters are at 1065 E. Hillsdale Blvd., Suite 400, Foster City, CA 94044. Additional information is available online at www.tefen.com.

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or
The Loomis Group Inc.
Bruce Hokanson, 360/574-4000
hokanson@loomisgroup.com

PUBLISHER NAME: Business Wire
COMPANY NAMES: *TEFEN USA
EVENT NAMES: *336 (Product introduction)
GEOGRAPHIC NAMES: *1USA (United States)
PRODUCT NAMES: *7372416 (Manufacturing, Distribution & Retailing Software)
INDUSTRY NAMES: BUS (Business, General); BUSN (Any type of business)
NAICS CODES: 51121 (Software Publishers)
?

02246710 Supplier Number: 57889349 (THIS IS THE FULLTEXT)

Asyst Technologies Introduces New Reticle Management System; Shrinking Geometries Create New Market for Reticle Manipulation and Protection Platforms.

Business Wire, p0482
Dec 1, 1999
Language: English Record Type: Fulltext
Document Type: Newswire; Trade
Word Count: 773

TEXT:

TOKYO--(BUSINESS WIRE)--Dec. 1, 1999--

In an announcement here at the opening of the SEMICON Japan 99, Asyst Technologies, Inc. (Nasdaq/NM:ASYT) today unveiled its new **Reticle Management System** (RMS) for use in **semiconductor** manufacturing. A platform for manipulating and protecting valuable **reticles** from particulate contamination and other potential sources of damage, the RMS is designed for use by **semiconductor** device manufacturers, **photomask suppliers** (**mask** houses) and original equipment manufacturers (OEMs).

In **semiconductor** manufacturing, the RMS can be used in the photolithography area to manipulate and identify **reticles** during the manufacturing process. **Mask** houses can use the RMS to manipulate **reticles** at the incoming inspection stage, while OEMs are able to use the RMS as an adaptive solution for production process tools that employ reticles.

Dennis Riccio, Asyst's senior vice president of Global Customer Operations, said, "We believe high-end applications in reticle management will account for a large portion of the growing substrate management business, which we estimate may reach $40 million next year. With the introduction of the RMS, we believe Asyst is poised to penetrate the new reticle management market."

"Historically, protecting reticles or masks from particulate contamination has not been an issue since the device feature sizes on the reticles are generally four times the size of those on the wafer," Riccio added. "But the reticles used to manufacture advanced 0.18-micron geometries have much smaller feature sizes. Thus, these reticles can be damaged during manufacture or use by the introduction of a even a single particle, by operator handling or misprocessing or by random electro-static discharge (ESD) damage. We believe the RMS can control these serious problems by fully automating the manipulation and identification of reticles."

The average cost of a complex 0.18-micron reticle is approximately $15,000 and multiple reticles are normally in use in semiconductor production fabs at all times. In particular, semiconductor foundries who specialize in producing many different device designs in smaller lots may have hundreds of reticles to protect at any given time in the production process. The RMS offers a way to protect these valuable assets, resulting in improved yields and reduced manufacturing costs.

In the case of mask houses, as the features on masks become smaller, the masks themselves become more expensive to manufacture and, therefore, even more important to protect. The RMS system is offered with an option for bright-light inspection -- a feature that improves manufacturing yields and provides a rapid return on investment.

RMS components include Asyst minienvironment and isolation technology, Asyst robotics for reticle handling, the Asyst Indexer front-end and Asyst graphical user interface software. The components are all modules designed and manufactured by Asyst, enabling the company to offer a cost-effective solution that can quickly and easily be configured or customized to suit customer needs. The RMS is currently available with an in-line R-Theta-Z robot working in concert with two or three input/output ports.

To address the special needs of mask houses and semiconductor manufacturers, the RMS opens, identifies and transfers reticles from various shipper boxes. These include: Hoya multi-reticle cassettes; Toppan

single reticle clam shells; ASML library/Asyst SMIF Pods; Asyst single-reticle SMIF Pods; and Nikon, SVGL and Canon boxes. A variety of options can be used due to the highly flexible design of the bulkhead-mountable in-line design.

The average selling price for a fully configured RMS system is between $250 - $300,000 depending on configuration. Multiple products have been installed at customer sites and the system is available for order from Asyst. The new RMS system will debut at the Asyst exhibit at SEMICON Japan, Dec. 1-3, 1999, at the Makuhari Convention Center, booth 6-A801.

About Asyst: Asyst Technologies, Inc. is a leading provider of Standard Mechanical Interface-based minienvironment and manufacturing automation systems that enable semiconductor manufacturers to protect customers' valued assets throughout the manufacturing process while increasing manufacturing productivity. Asyst offers a broad range of 200 mm and 300 mm products that enable the Company to provide semiconductor manufacturers and Original Equipment Manufacturers automated manufacturing solutions for the transfer of wafers and information between the process equipment and the fab line. Asyst's homepage is located on the World Wide Web at http://www.asyst.com

Except for statements of historical fact, the statements in this press release are forward-looking. Such statements are subject to a number of risks and uncertainties that could cause actual results to differ materially from the statements made. These factors include, but are not limited to, general economic conditions, semiconductor industry cycles, risks associated with the acceptance of new products and product capabilities and other factors more fully detailed in the Company's most recent S-3 Registration Statement.

PUBLISHER NAME: Business Wire
COMPANY NAMES: *Asyst Technologies Inc.
PRODUCT NAMES: *3559581 (Semiconductor Production Equip)
INDUSTRY NAMES: BUS (Business, General); BUSN (Any type of business)
SIC CODES: 3559 (Special industry machinery, not elsewhere classified)
NAICS CODES: 333295 (**Semiconductor** Machinery Manufacturing)
TICKER SYMBOLS: ASYT
?

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Set     Items   Description
S1          7   AU='WIESLER, M.':AU='WIESLER, O.L.'
S2          5   AU='MARIANO, T.':AU='MARIANO, THOMAS MICHAEL'
S3          2   S1:S2 AND (RETICLE? OR MASK? OR WAFER? OR PHOTOMASK?OR RET-
              ICULE?)
S4         20   (WIESLER(2N)OREN OR MARIANO (2N)THOMAS)
S5          2   S4 AND (RETICLE? OR MASK? OR WAFER? OR PHOTOMASK?OR RETICU-
              LE?)
S6        134   CO=PRI AUTOMATION
S7        134   CO='PRI AUTOMATION'
S8        118   S7 AND (RETICLE? OR MASK? OR WAFER? OR PHOTOMASK?OR RETICU-
              LE?)
S9         20   S8 AND (DATA OR DATABASE?)
S10        18   RD (unique items)
S11        18   S10 NOT PY>2000
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File  35:Dissertation Abs Online 1861-2004/May
         (c) 2004 ProQuest Info&Learning
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         (c) 2004 Business Wire.
File 810:Business Wire 1986-1999/Feb 28
         (c) 1999 Business Wire
File   9:Business & Industry(R) Jul/1994-2004/Jun 07
         (c) 2004  The Gale Group
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and Controlling Device Manufacturing); 51121 (Software Publishers); 334413 (Semiconductor and Related Device Manufacturing); 32512 (Industrial Gas Manufacturing); 33451 (Navigational, Measuring, Electromedical, and Control Instruments Manufacturing); 334111 (Electronic Computer Manufacturing); 333911 (Pump and Pumping Equipment Manufacturing); 334516 (Analytical Laboratory Instrument Manufacturing); 334513 (Instruments and Related Products Manufacturing for Measuring, Displaying, and Controlling Industrial Process Variables)
TICKER SYMBOLS: APD; BRKS; MTL; OSIX; PSX
SPECIAL FEATURES: LOB; COMPANY

11/9/3 (Item 3 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)

03840322 Supplier Number: 45495508 (THIS IS THE FULLTEXT)
PRI To Automate Taiwanese Chip Manufacturing Plant 04/25/95
Newsbytes, pN/A
April 25, 1995
Language: English Record Type: Fulltext
Document Type: Newswire; General Trade
Word Count: 673
TEXT:
BILLERICA, MASSACHUSETTS, U.S.A., 1995 APR 25 (NB) -- In a deal billed as the first to be forged between an Asian-based chip maker and a US semiconductor manufacturing specialist, PRI Automation Inc. has won an $11 million order from Model Vitelic, Taiwan.

The contract also departs from tradition by calling for automation of a six -inch **wafer** manufacturing facility, instead of the eight- inch **wafer** plants that are the usual candidates for automation, said Mitchell G. Tyson, PRI's president and chief operating officer, in an interview with Newsbytes.

Tyson told Newsbytes that, under the deal, PRI will install an automated materials handling system -- supplying "monorail-like" materials transport in the cleanroom environment -- to Model Vitelic's **wafer** processing facility in Hsinchu, Taiwan.

In the US, Billerica, Massachusetts-based PRI has won ten of its last 11 bids against Baifuku, a Japanese company that represents its chief competition, according to Tyson.

"Prior to our entry, Baifuku had 100 percent of the (world) market. This is the first time we've been able to take an order (over) Baifuku in Asia. And for us, the ability to compete in Asia m[illegible] our total market has just effectively doubled," asserted the

As a region, he added, Taiwan and nearby Sing[illegible] in terms of semiconductor manufacturing, increasin[illegible] automation by 60 percent, in contrast to 20 percen[illegible]

As a result of its new relationship with Mose[illegible] establish an expansion office in Taiwan, and will[illegible] Pacific Rim (Pac Rim) office in Singapore by the e[illegible] reported.

Mosel Vitelic is a $250 million company that [illegible] (DRAM), video RAM (VRAM), and static RAM (SRAM) memory chips [illegible] **data** storage, telecommunications, printer, graphics accelerator, and CD-ROM applications, according to Tyson.

PRI Automation

Although new plants are now being built for eight-inch **wafers** , the six-inch **wafers** used at Hsinchu typify **wafer** technology at many existing plants worldwide, Newsbytes was told.

"Eight-inch **wafers** are regarded as requiring automation because they are heavier, and require more space. But six-inch **wafers** are candidates for automation, as well," the company chief maintained.

PRI, he said, will automate Mosel Vitelic's existing six-inch **wafer** plant, plus an expansion facility now being built, using more than 1,000 feet of AeroTrak monorail to link "stockers," or materials storage bins, as well as to transport "intelligent cars" that will carry the **wafers** between the stockers.

"A semiconductor fabrication facility is laid out somewhat like a

spine with ribs. There is a central corridor, and off of that, a series of perpendicular corridors. Along these horizontal corridors are "bays' for up to 400 different process tools," Tyson explained.

"In an automated facility, when an operator finishes performing a process step at a bay, the operator will place the **wafer** in a stocker. A robot inside the stocker will detect the **wafer** , lift it up, and place it in a monorail car. The car will then go to where the next process step is being performed, drop off the **wafer** , and wait for the **wafer** there," he continued.

The monorail, he noted, hangs suspended from the ceiling, above the operator level. "It's very flexible. We can route it, and create paths. And like all our products, it's cleaner than the cleanest surgical suite. Because the slight particle of dust can short out a circuit, meaning millions of dollars lost for the semiconductor manufacturer," Tyson contended.

Founded in 1982, PRI is currently concentrating exclusively on the semiconductor industry, according to the company chief. Over the past three years, company revenues have grown at the rate of 80 percent annually, he added.

"But we have formed a group inside the company that's looking for opportunities outside of semiconductors, and that group has been looking at manufacturing of flat panel displays, as well as some applications in pharmaceuticals," the PRI president revealed.

(Jacqueline Emigh/19950424/Reader Contact: PRI Automation, 508-663-8555; Press Contact: Michelle Goodall or Pamela Hamilton, Schwartz Communications for PRI, 617-431-0770)

PUBLISHER NAME: Newsbytes News Network
COMPANY NAMES: Model Vitelic; **PRI Automation**
EVENT NAMES: *430 (Capital expenditures); 610 (Contracts & orders received)
GEOGRAPHIC NAMES: *9TAIW (Taiwan)
PRODUCT NAMES: *3674000 (Semiconductor Devices); 1629290 (Industrial Nonbldg Constructn NEC)
INDUSTRY NAMES: BUSN (Any type of business); CMPT (Computers and Office Automation); TELC (Telecommunications)
NAICS CODES: 334413 (Semiconductor and Related Device Manufacturing); 23493 (Industrial Nonbuilding Structure Construction)
SPECIAL FEATURES: LOB; COMPANY

11/9/4 (Item 4 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)

03815578 Supplier Number: 45445077 (THIS IS THE FULLTEXT)
MATERIAL HANDLING UPDATE: PRI IS IN THE CHIPS
Manufacturing Automation, v4, n7, pN/A
April, 1995
ISSN: 1060-2712
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 521
TEXT:
PRI Automation, Inc (NASDAQ: PRIA) (Billerica, MA) has been awarded a multi -year, $10 million order from Integrated Device Technology, Inc (NASDAQ: IDTI) (Santa Clara, CA) for a factory automation system that will be installed at IDT's new semiconductor fabrication facility under construction in Hillsboro, OR. Under the terms of the agreement, PRI will design and install an integrated transportation, storage, and management system- -including monorails, stockers, and control subsystems--used for moving eight -inch silicon **wafers** through the front end of the semiconductor manufacturing process performed at the world-class facility, which will be the first eight -inch **wafer** fab built by IDT.

The contract calls for a phased approach to installing PRI's equipment and related services, beginning in midyear. The IDT award represents the

ninth full fab contract that PRI has been awarded in the past two years; and the value of such contracts totals $100 million.

"PRI is pleased to be participating in IDT's expansion," commented Mitchell Tyson, president and COO of PRI Automation. "This venture will enable us to broaden our strategy of enriching the production facilities of both mid-size and specialty semiconductor producers."

IDT, which has about 2,800 employees worldwide, designs, manufactures, and markets CMOS VLSI integrated circuits for a variety of growth markets, including desktop computer, workstation/server, **data** communications, and office automation. The company's products address the following synergistic areas: high-speed SRAMs; RISC microprocessors; and high-performance logic.

PRI, which issued an initial public offering last October, designs, develops, and manufactures systems that automate the transport, storage, and handling of silicon **wafers** that are used to manufacture microprocessors, memory chips, and other semiconductor components. The company also offers system integration, factory simulation, project management, and automation support services to its customers, which include leading semiconductor companies.

Global revenues for automated electrified monorails (AEMs) are forecast to increase at a 9.2% compound annual rate to total $247.9 million in 1999, from $133.9 million in 1992, according to Frost & Sullivan's World Intelligent Material Handling Markets report (828-10). Revenues for 1995-1997 are pegged at $168.5 million, $184.2 million, and $202.5 million, respectively. Worldwide unit shipments of AEMs are predicted to rise at a 7.1% compound annual rate to reach 11,779 in 1999, as opposed to 7,269 in 1992. Unit shipments for 1995-1997 are projected at 8,709, 9,340, and 10,059, respectively.

In 1995, the projected geographical distribution of the total revenues for AEMs is (all figures are rounded): US--15.3%; Europe--41.6%; and Asia/ROW- -43.0%. In 1999, the distribution will be: US--14.1%; Europe--42.5%; and Asia/ROW--43.4%.

In 1995, the projected end-user industry distribution of the global revenues for automated electrified monorails is: automotive--30.1%; aerospace/defense- -11.9%; heavy engineering--13.0%; pharmaceutical--3.6%; process (including food & beverage)--12.7%; electronics--9.7%; consumer products and wholesale distribution--15.3%; and "other" (including miscellaneous manufacturing and service industries)--3.7%. In 1999, the distribution is expected to be (all figures are rounded): automotive--32.6%; aerospace/defense--9.6%; heavy engineering--13.9%; pharmaceutical--3.7%; process--13.1%; electronics--9.7%; consumer products and wholesale distribution--13.6%; and "other"--3.9%.

PUBLISHER NAME: Vital Information Publications
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INDUSTRY NAMES: BUSN (Any type of business); CMPT (Computers and Office Automation)
NAICS CODES: 334413 (Semiconductor and Related Device Manufacturing)
TICKER SYMBOLS: IDTI
SPECIAL FEATURES: COMPANY

11/9/6 (Item 1 from file: 810)
DIALOG(R)File 810:Business Wire

0944235 BW0318

PRI AUTOMATION : **PRI Automation to Acquire Promis Systems; Semiconductor Manufacturers to Benefit From Integrated** Wafer **-Flow Solution**

November 24, 1998

Ticker Symbol: PRIA
Byline: Business Editors/High Tech Writers
Dateline: BILLERICA, Mass.
Time: 21:33 PT
Word Count: 1233

BILLERICA, Mass.--(BUSINESS WIRE)--Nov. 24, 1998--PRI Automation, Inc. (Nasdaq:PRIA), the leader in semiconductor factory automation, today announced that it has reached a definitive agreement to acquire Promis Systems Corporation Ltd. (TSE:PSW), the leading developer of Manufacturing Execution Systems (MES) for semiconductor and precision electronics manufacturers. The acquisition, which will be accounted for as a pooling of interests, is expected to be completed during the first quarter of 1999, subject to, among other things, regulatory approvals and approval of the shareholders of Promis Systems Corporation Ltd.

Under the terms of the definitive agreement, PRI will acquire Promis in a stock-for-stock acquisition. The price per share will be fixed at CDN$6.65, as long as PRI Automation's average stock price during a period prior to closing is within a specified collar. At Monday's closing prices, the exchange ratio was 0.1691 shares of PRI stock for each share of Promis stock.

In connection with the execution of the definitive agreement, Promis granted PRI a contingent option to purchase up to 19.9% of the common shares of Promis at a price of US$4.29 (CDN$6.65) per share. The option would only become exercisable if the definitive agreement is terminated in certain circumstances.

Mitch Tyson, president and chief executive officer of PRI Automation said, "The acquisition of Promis Systems significantly enhances PRI Automation's **wafer** flow solution. Promis Systems brings market leadership, a strong technology direction in Promis Encore!(R), and proven software management expertise. Consistent with our established strategy, we now offer the only comprehensive, integrated **wafer** logistics solution. This capability enables semiconductor manufacturers to further increase profitability by reducing cycle times, accelerating fab start-up, and improving manufacturing flexibility."

"We believe this transaction is the best way to maximize value for shareholders and customers of Promis Systems," said Ian McKinnon, president and chief executive officer of Promis Systems. "PRI is now extraordinarily well positioned to serve the semiconductor industry worldwide with:

-- Leadership customers in every segment of the market including Logic, Foundry/ASIC, DRAM, assembly and test;
-- Increased expertise including over 250 software professionals;
-- The only comprehensive **wafer** flow solution with leading products in MES, Automated Material Handling Systems (AMHS), Advanced Planning and Scheduling (APS), and tool automation; and
-- An expanded direct sales and support presence in every major market worldwide.

Simply put, only PRI is able to deliver an integrated **wafer** logistics management system that optimizes overall factory effectiveness." Ian McKinnon will become vice president and general manager of PRI's Software Division, based in Toronto, and will be responsible for all of the company's software products, including TransNet(TM), PRI's material control software, and the Leverage suite of advanced planning and scheduling software products from Interval Logic, a subsidiary of PRI. In his new role, McKinnon will report directly to Mitch Tyson.

Dan Hutcheson, president of VLSI Research commenting on the announcement stated, "This acquisition makes a lot of sense and addresses the goals regarding factory integration outlined in the 1997 SIA Roadmap. PRI has been very clear about its vision of delivering complete factory automation solutions, and the acquisition of Promis Systems supports that strategy. This is a great combination of two

industry leaders, coming together to offer their customers more value."

Moving Up the Value Chain

PRI's integrated **wafer** flow solution, including Promis Systems' MES software, manages and enhances all of the manufacturing systems -- whether information or automation -- from the tools to the Enterprise Resource Planning system. With access to real-time operational **data** through PROMIS(R) and the ability to develop workflow schedules through Leverage(TM) for Scheduling, PRI can now optimize **wafer** flows based on real-time shop floor events. Mitchell Weiss, vice president strategy and technology, PRI Automation said, "Our strategy is to offer a comprehensive **wafer** logistics management system delivering 'out-of-the-box' integration of MES, scheduling, planning, material control software, and automated material handling systems. By orchestrating **wafer** logistics for our customers, we enable them to focus on the critical issues of product and process optimization."

About Promis Systems

Promis Systems develops and markets manufacturing execution systems and automation solutions to semiconductor and precision electronics manufacturers worldwide. MES systems plan, monitor, automate, and control production. MES systems contain and control the key process and routing **data** in the factory, with its overriding mission of ensuring coordination among all the elements of manufacturing: labor, equipment, tooling (**reticles** , for example), processes/specifications, and materials. The PROMIS(R) software application and its modules, combined with the Promis Encore! suite of plug-and-play Windows NT products, provide a robust MES and automation framework for semiconductor and precision electronics manufacturing. Promis products are installed at over 270 of the world's leading manufacturing sites in 25 countries. The Company is headquartered in Toronto, Ontario, Canada, and maintains sales and support offices through North America, Europe, and Asia Pacific. For more information visit the Promis Systems Web site at www.promis.com.

About PRI Automation

PRI Automation, Inc., headquartered in Billerica, Mass., is a leading global supplier of advanced factory automation systems that enhance the competitiveness of semiconductor manufacturers and OEM process tool manufacturers. PRI is the only company to provide a tightly integrated and flexible hardware and software solution that optimizes the flow of **wafers** throughout the fab. The company currently has thousands of systems installed at approximately one hundred locations throughout the world. For more information visit PRI's Web site at www.pria.com

This release includes forward-looking statements, including, without limitation, statements concerning the company's future revenues and expenses, management's plans and objectives for future operations, the effect of any consolidation or restructuring of operations on the company's future profitability and the effects of a continued downturn in the semiconductor manufacturing industry, and other matters not limited to historical facts. These forward-looking statements are subject to risks and uncertainties that could cause actual results to differ materially from those expressed or implied by such statements. Such risks and uncertainties include, but are not limited to (i) uncertainty that the acquisition will be completed and that, if completed, will produce the benefits and synergies that PRI expects, (ii) the cyclicality of the semiconductor industry and the possibility of a prolonged downturn in such industry, (iii) uncertainties affecting Asian markets and currencies, (iv) the effects of possible delays in the expected transition to 300mm **wafer** technology, (v) the difficulty of reducing costs and expenses to the extent necessary in light of current business levels, and other factors identified in the company's annual report on Form 10-K for fiscal year 1997 and its quarterly reports on Form 10-Q for fiscal year 1998, as filed with the Securities and Exchange Commission. The company assumes no obligation to update this information.

Note to Editors: When referring to the Company, please use Promis Systems, or Promis Systems Corporation. When referring to the

products, please use PROMIS (all caps) and/or Promis Encore! (with exclamation point).

PROMIS and Promis Encore! are registered trademarks of Promis Systems Corporation. TransNet is a trademark of PRI Automation, Inc. Leverage and Leverage for Scheduling are trademarks of Interval Logic Corporation. All other trademarks are those of their respective owners.

/sf

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KEYWORD: MASSACHUSETTS
INDUSTRY KEYWORD: COMPUTERS/ELECTRONICS COMED MERGERS/ACQ

11/9/7 (Item 2 from file: 810)

0942318 BW0197

PRI AUTOMATION : PRI Automation Reports Fourth-quarter and Fiscal 1998 Results

November 19, 1998

Ticker Symbol: PRIA
Byline: Business Editors
Dateline: BILLERICA, Mass.
Time: 13:01 PT
Word Count: 1202

BILLERICA, Mass.--(BUSINESS WIRE)--Nov. 19, 1998--PRI Automation, Inc. (Nasdaq: PRIA), the leader in semiconductor factory automation, today reported financial results for the fourth quarter and fiscal year ended September 30, 1998.

"Our results for the fourth quarter and the fiscal year reflect the impact of the prolonged downturn in the industry," noted Mitch Tyson, president and chief executive officer, PRI Automation. "But we believe that this may be the bottom of the cycle and that business conditions are beginning to improve."

Net revenue for the fiscal year was $178.2 million, compared with $213.2 million a year earlier, a decline of 16%. Excluding special charges and adjusted on a pro forma basis, to reflect the conversion of Equipe Technologies from an S-corporation to a C-corporation for income tax purposes, net income for the year was $0.7 million, or $0.04 per share, compared with the prior year's net income of $22.9 million, or $1.14 per share. Net revenue for the fourth quarter was $27.6 million, compared with $63.6 million for the fourth quarter of fiscal 1997. Excluding special charges, the company reported a net loss for the quarter of $4.0 million, or $(0.20) per share on a diluted basis. This compared with net income of $6.9 million, or $0.34 per share, for the same period last year on a pro forma basis, for the conversion of Equipe Technologies' tax status. Sequentially, cash and

marketable securities rose from $39.1 million to $48.2 million during the fourth quarter.

In the fourth quarter, the company recorded special charges of $7.0 million, net of taxes, or $(0.36) per share, for costs related to inventory and warranty provisions, severance compensation, and plant consolidations. For the fiscal year, the company recorded special charges of $25.8 million, net of taxes -- $12.8 million related to the acquisition of Interval Logic and Equipe Technologies, and $13.0 million related to restructuring and other activities.

"We are continuing to improve our cash position and reduce our cost structure as we develop our next-generation products, expand our **wafer** flow solutions, and strengthen our position for the upturn," said Tyson. "During this period we have been able to gain market share and believe that we are positioned to be stronger and more profitable when the recovery comes."

Tyson continued, "Our Factory Automation Systems division has not lost a single factory automation order in the past year, and we have grown our worldwide market share, most notably in Taiwan and Singapore, where we are now the factory automation supplier of choice for the world's leading foundries. We are seeing increased activity among our **reticle** management systems as fabs increase the number and volume of **reticles** they must handle. Our Interval Logic subsidiary is shipping its advanced planning and scheduling software, and customers will soon be benefiting from the productivity gains these solutions bring to capacity planning and work-flow scheduling. The Equipe division is growing its share in the vacuum **wafer** -handling market by winning new customer orders for its vacuum cluster platform products."

Tyson concluded, "We believe that we are seeing an increase in business activity in both 200mm and 300mm sectors and we hope this activity will lead to an improvement in bookings and revenue in our FY'99."

About PRI Automation

PRI Automation, Inc., with headquarters in Billerica, Massachusetts, is the leading global supplier of advanced factory automation systems that enhance the competitiveness of semiconductor manufacturers and OEM equipment suppliers. PRI is the only company to provide a tightly integrated and flexible hardware and software solution that optimizes the flow of **wafers** throughout the fab. The company currently has more than 1,600 systems installed at approximately 100 locations worldwide. For more information, visit PRI's Web site at http://www.pria.com.

This release includes forward-looking statements, including, without limitation, statements concerning the company's future revenues and expenses, management's plans and objectives for future operations, the effect of any consolidation or restructuring of operations on the company's future profitability and the effects of a continued downturn in the semiconductor manufacturing industry, and other matters not limited to historical facts. These forward-looking statements are subject to risks and uncertainties that could cause actual results to differ materially from those expressed or implied by such statements. Such risks and uncertainties include (i) the cyclicality of the semiconductor industry and the effects of a prolonged downturn in such industry, (ii) uncertainties affecting Asian markets and currencies, (iii) the effects of possible delays in the expected transition to 300mm **wafer** technology, (iv) the difficulty of reducing costs and expenses to the extent necessary in light of current business levels, and other factors identified in the company's annual report on Form 10-K for fiscal year 1997 and its quarterly reports on Form 10-Q for fiscal year 1998, as filed with the Securities and Exchange Commission. The company assumes no obligation to update this information.

PRI Automation, Inc.
Condensed Consolidated Statements of Operations
(In thousands, except per share **data**)

	Three Months Ended		Year Ended	
	9/30/98	9/30/97	9/30/98	9/30/97

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Demer IR Counsel, Inc.
Mary McGowan, 925/938-2678
KEYWORD: MASSACHUSETTS
INDUSTRY KEYWORD: COMPUTERS/ELECTRONICS COMED EARNINGS
Today's News On The Net - Business Wire's full file on the Internet
with Hyperlinks to your home page.
URL: http://www.businesswire.com
>

11/9/13 (Item 8 from file: 810)
DIALOG(R)File 810:Business Wire

0666161 BW1117

PRI AUTOMATION : **Pri Automation names two to Tool Automation Systems Division**

January 28, 1997

Ticker Symbol: PRIA
Byline: Business/Technology Editors
Dateline: BILLERICA, Mass.
Time: 05:32 PT
Word Count: 580

BILLERICA, Mass.--(BUSINESS WIRE)--Jan. 28, 1997--
Dan Peterson to Vice President of Sales and Marketing and
Raymond Sawtelle to Director Of Manufacturing
PRI Automation, Inc. (NASDAQ: PRIA), a world leader in developing, marketing and implementing full-factory automation systems for semiconductor manufacturers, announced today the appointment of two executives to the Tool Automation Systems (TAS) Division: Dan Peterson to Vice President of Sales and Marketing, and Raymond Sawtelle to Director Of Manufacturing. Both are based at PRI's Billerica, Mass., headquarters and report to Jim Costa, General Manager of TAS.
Dan Peterson
As Vice President of Sales and Marketing, Peterson is responsible for expanding the Company's product portfolio that address the needs of the 300mm process tool OEMs so they can easily and cost-effectively integrate their products into an automated 300mm fab; and growing the business for current products that address fab-specific and applications-specific process tool automation needs. Peterson has 16 years of sales and marketing experience in the semiconductor capital equipment industry. Previously, he worked for Applied Materials as a Site Operations Manager and Schlumberger Technologies as Director of Marketing and Sales: Automated Systems Group, among other companies. Peterson received a B.S. in Electrical Engineering from the University of Massachusetts and is a member of the Tau Beta Pi National Engineering Honor Society.
Raymond Sawtelle
As Director of Manufacturing, Sawtelle is directly responsible for TAS' materials organization (purchasing, production control and planning), manufacturing (system level and sub-assembly), project management, manufacturing engineering, documentation control, quality assurance and technical publications.
Sawtelle has more than 20 years of management experience in manufacturing. Most recently, he served as Vice President of Customer Service, Quality Assurance and Program Management for Sky Computers Inc., Director of Manufacturing for Monitronix Inc., and Director of Program Management for Raster Technologies. Sawtelle received an Associate of Business Administration from Dean Junior College. He also attended the Control **Data** Institute, and served four years in the United States Air Force. Sawtelle is a member of

the American Society for Quality Control.

"The growing adoption of factory-wide automation has stimulated a need for new tool automation solutions that integrate process tools with intrabay and interbay automation systems," said PRI's President Mitch Tyson. "Dan's and Ray's extensive management experience in the semiconductor and manufacturing industries will help grow our TAS division which focuses on this opportunity."

About TAS

The TAS division manufactures PRI's current tool automation products for CMP, diffusion furnace, spray tool, PECVD, and wet bench processes. TAS also develops new tool products for 200mm and next generation 300mm silicon **wafers** and flat panel display (FPD) substrates, and markets PRI's automated laser marking system for FPD manufacturers.

About PRI Automation

PRI Automation, Inc., headquartered in Billerica, Mass., is the leading U.S. supplier of factory automation systems that serve the needs of large, mid-sized and specialty semiconductor manufacturers and the flat panel display industry. The Company combines advanced robotics technology with material handling software to automate the complex processes of integrated circuit manufacturing. PRI's systems-which include overhead monorails, **wafer** stockers, **reticle** stockers, tool automation systems, material control software, and factory simulation and other services-maximize **wafer** yield and equipment utilization in a wide range of semiconductor manufacturing environments, while providing efficient work-in-process logistics to optimize manufacturing throughput. PRI currently has more than 1,400 systems, including 30 full-fab automation systems, installed at approximately 100 locations worldwide.

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KEYWORD: MASSACHUSETTS
INDUSTRY KEYWORD: COMED COMPUTERS/ELECTRONICS MANAGEMENT CHANGES

11/9/14 (Item 9 from file: 810)

0601780 BW1225

PRI AUTOMATION : **PRI wins $15.9-million contract to automate Siemens Semiconductor fab in U.K.; First full-fab automation for Siemens**

July 09, 1996

Ticker Symbol: PRIA
Byline: Business/Technology Editors
Dateline: BILLERICA, Mass.
Time: 08:19 PT
Word Count: 404

BILLERICA, Mass.--(BUSINESS WIRE)--July 9, 1996--PRI Automation, Inc. (NASDAQ: PRIA), a world leader in developing, marketing and implementing full-factory automation systems for semiconductor manufacturers, announced today that it has received a $15.9-million order from Siemens Semiconductor for Siemens' new North Tyneside, United Kingdom, manufacturing facility.

PRI will install more than 20 stockers, an AeroTrak overhead monorail system, and TransNet, fully integrated material control software, to automate the interbay transport, tracking and delivery of 200mm silicon **wafers** in SMIF-pods.

"PRI has worked with Siemens in the past, primarily on interbay

automation applications for the Regensburg and Siemens joint venture in Essonnes, France," said PRI President Mitch Tyson. "We are delighted about our first full-fab system order from Siemens, and look forward to bringing the efficiencies of fab-wide automation to their North Tyneside facility."

"Siemens selected PRI for the factory-wide automation system in the new U.K. fab, taking full advantage of the automation technology," explained Siemens North Tyneside Automation Manager Wolfgang Mayr. "Our most important requirement was that the system be expandable." PRI expects to install the system in early 1997.

This order is in addition to several other recent full-fab automation system orders for European customers (totaling approximately $20 million) that PRI announced in April 1996.

PRI Automation, Inc., headquartered in Billerica, Mass., is the leading U.S. supplier of factory automation systems that serve the needs of large, mid-sized and specialty semiconductor manufacturers and the flat panel display industry. The Company combines advanced robotics technology with material handling software to automate the complex processes of integrated circuit manufacturing. PRI's systems -- which include overhead monorails, **wafer** stockers, **reticle** stockers, material control software, and factory simulation and other services -- maximize **wafer** yield and equipment utilization in a wide range of semiconductor manufacturing environments, while providing efficient work-in-process logistics to optimize manufacturing throughput. PRI currently has more than 1,000 systems, including 25 full-fab automation systems, installed at approximately 100 locations worldwide.

Siemens Semiconductor Group is a leading supplier of electronic components for automotive, communications, consumer electronics, **data** processing embedded control and memory applications worldwide. Headquartered in Munich, Germany, Siemens Semiconductor Group employs 15,900 and had worldwide sales exceeding $2.9 billion in the 1994/95 fiscal year.

AeroTrak and TransNet are trademarks of PRI Automation.

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KEYWORD: MASSACHUSETTS
INDUSTRY KEYWORD: COMPUTERS/ELECTRONICS COMED INTERACTIVE/MULTIMEDIA/INTERNET

11/9/15 (Item 10 from file: 810)

0601238 BW1112

PRI AUTOMATION : **PRI Automation creates new software division and enters material control software market with TransNet; Responding to customer demand, PRI develops its own software solution to Provide 'One-Stop Shopping' for semiconductor manufacturers**

July 08, 1996

Ticker Symbol: PRIA
Byline: Business/Technology Editors
Dateline: BILLERICA, Mass.
Time: 06:26 PT
Word Count: 696

BILLERICA, Mass.--(BUSINESS WIRE)--July 8, 1996--PRI Automation,

Inc. (NASDAQ: PRIA), a world leader in developing, marketing and implementing full-factory automation systems for semiconductor manufacturers, today introduced the semiconductor industry's first Windows-based, totally integrated material control software for fabs: TransNet.

Based on an open Windows NT platform, TransNet is a flexible, scalable system that tightly integrates with Manufacturing Execution Systems (MES) software, as well as with PRI's hardware on the fab floor, such as the Company's stockers and AeroTrak overhead monorail transport system. For the first time semiconductor manufacturers can contract with one OEM--PRI--for a complete fab automation system, including all software and hardware support.

TransNet is the first product to emerge from PRI's newly-created Software Division, an internal group charged with providing complete integration services to satisfy PRI's customers' "one-stop shopping" requirements; driving software business strategies and practices; managing third-party relationships with other software vendors; and providing enabling software technology for PRI. PRI's Software Division will also develop new high-level software products, the first of which is TransNet.

"TransNet is the next logical step for PRI in providing full-factory automated material handling solutions," said PRI's president Mitch Tyson. "Our expertise is in material handling and software integration -- experience that makes PRI uniquely qualified to develop the optimal material control software for semiconductor manufacturers."

"Although PRI has always been able to integrate third-party material control software, time and again customers have asked us to provide a fully-integrated, top-to-bottom, cost-effective solution for material handling," said Doug Lawson, vice president of Software for PRI. "TransNet is currently being beta tested by leading semiconductor manufacturers worldwide and has been extremely well received."

Because TransNet runs on a networked Windows platform, fab managers can access **data** from any point in the system -- be it on the fab floor at a PRI stocker or remotely from an NT-based workstation in an office. Users can also create customizable reports directly from the software. TransNet is an open solution that is fully-compatible with all the leading suppliers of Manufacturing Execution Systems. TransNet's architecture directly interfaces with the fab's host system and with PRI's factory automation hardware to reduce integration time and more efficiently manage material transfer throughout the fab.

The Software Division has migrated all of PRI's hardware controllers to Windows NT to complete the main product set. The Company has also transitioned to an Ethernet-based network, which will enhance the speed of information transfer and allow customers to grow their PRI automation systems to larger scales. "Integration is much easier when an automation system is completely TransNet-based," said Lawson. "TransNet's remote access features allow for more effective diagnostics and service. The bottom line is a more reliable, easier-to-use automation system that costs less to set up and maintain."

TransNet will begin shipping during Q3 1996, and will be demonstrated publicly for the first time at SEMICON/West '96 (July 15-18, 1996, San Francisco, Calif.) at PRI's booth 1826.

PRI's Software Division will be led by Lawson (formerly vice president of engineering). It will have its own engineering group and utilize PRI's central sales/marketing resources.

PRI Automation, Inc., headquartered in Billerica, Mass., is a leading global supplier of factory automation systems that serve the needs of large, mid-sized and specialty semiconductor manufacturers and the flat panel display industry. The Company combines advanced robotics technology with material handling software to automate the complex processes of integrated circuit manufacturing. PRI's systems -- which include overhead monorails, **wafer** stockers, **reticle** stockers, material control software, and factory simulation and other

services -- maximize **wafer** yield and equipment utilization in a wide range of semiconductor manufacturing environments, while providing efficient work-in-process logistics to optimize manufacturing throughput. PRI has over a decade of success in automating material handling in new and existing fabs. The Company currently has more than 1,000 systems, including more than 25 full-fab automation systems, installed at approximately 100 locations worldwide.

Editor's Note: Screen shots of TransNet are available for download at http://www.schwartz-pr.com/pri

AeroTrak and TransNet are trademarks of PRI Automation, Inc.

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KEYWORD: MASSACHUSETTS
INDUSTRY KEYWORD: COMPUTERS/ELECTRONICS COMED INTERACTIVE/MULTIMEDIA/INTERNET TRADESHOW

11/9/17 (Item 12 from file: 810)

DIALOG(R)File 810:Business Wire

0476552 BW1082

PRI AUTOMATION : **PRI enters Asian semiconductor fab market with $11 million contract; Leading U.S. factory automation supplier wins bid for Mosel Vitelic's automated manufacturing facility**

April 10, 1995

Ticker Symbol: PRIA
Byline: Business Editors
Dateline: BILLERICA, Mass.
Time: 05:56 PT
Word Count: 578

BILLERICA, Mass.--(BUSINESS WIRE)--April 10, 1995--PRI Automation Inc. (NASDAQ:PRIA) announced today it has won an $11 million order from Taiwan-based Mosel Vitelic, marking the company's entry into the Asian semiconductor manufacturing market.

PRI will provide an interbay automated materials handling system for 6" **wafers** to be installed in the existing sub half-micron **wafer** processing facility in Hsinchu, Taiwan.

"PRI is the leading supplier of factory automation systems for semiconductor manufacturers in the U.S. and also has a strong presence in Europe," stated Mitchell G. Tyson, president and chief operating officer. "This contract with Mosel Vitelic is significant because it is our first for the Pacific Rim, the fastest-growing region for the semiconductor industry, and because it is a 6" fab -- pointing to the continuing potential in existing fabs."

"PRI's integrated transportation, storage and management system will be instrumental in improving the efficiency of our Hsinchu facility," said Mosel Vitelic President Hung Chiu Hu. "Mosel Vitelic is expanding the 6" **wafer** fab to satisfy increased demand for its products and requires state-of-the-art automation technology to meet its production objectives. We were impressed with the flexibility of PRI's solution and the company's ability to retrofit the system in our existing facility.

"PRI made a strategic decision to expand its sales efforts to Asia because it represents approximately half the world's current capital spending on semiconductor manufacturing equipment," said Bob Postle, vice president of marketing and sales. "Our alliance with

Mosel Vitelic, a leading supplier of high-volume memory products, represents the first time an American company is supplying factory automation equipment in the Asian semiconductor market. We look forward to a long-term relationship with Mosel Vitelic."

PRI will automate Mosel Vitelic's existing 6" **wafer** facility, as well as an expansion currently being built, to maximize efficiency in the manufacturing process while minimizing the floor space needed for **wafer** storage. Using more than 1,000 feet of AeroTrack monorail, PRI will link stockers with intelligent cars that transport and store the **wafers** during chip processing. PRI will also provide complete software integration for the fab's material control system.

Mosel Vitelic, with revenues of $250 million (U.S.) in 1994, serves the **data** storage, telecommunications, computer peripheral and printer markets with high-volume memory products, while supplying innovative niche products for graphics accelerator and CD-ROM applications. In addition to DRAM and VRAM, Mosel Vitelic's principle products include SRAMs. The company applies state-of-the-art design techniques to manufacture competitive high-volume specialty products for the high-performance PC and workstation marketplace. This strategy provides economies of scale in manufacturing and sales and allows Mosel Vitelic to insulate itself form the more vulnerable main-memory market. Mosel Vitelic also has a facility in San Jose, Calif.

PRI Automation, headquartered in Billerica, Mass., is the leading U.S. supplier of factory automation systems to the semiconductor industry. The company combines advanced robotics technology with materials handling software to automate the complex process of integrated circuit manufacturing. PRI's systems maximize **wafer** yield and equipment utilization while providing highly flexible solutions in a wide range of manufacturing environments. PRI has won 90% of contracts for large automated materials handling systems awarded in the U.S. in the past two years, and currently has more than 1,000 systems installed at approximately 100 locations worldwide.

AeroTrak is a trademark of PRI Automation Inc.

CONTACT: PRI Automation Inc., Billerica
Marianne Russell (media), 508/670-4270 ext. 3047
John Schickling (investors), ext. 3002
or
Schwartz Communications Inc., Wellesley, Mass.
Pamela Hamilton, 617/431-0770 ext.222
Michelle Goodall, ext. 215
KEYWORD: MASSACHUSETTS
INDUSTRY KEYWORD: COMED COMPUTERS/ELECTRONICS

11/9/18 (Item 13 from file: 810)

0467723 BW0216

PRI AUTOMATION **IDT: PRI Automation wins $10 million order from Integrated Device Technology; Leading factory automation supplier to maximize efficiency of new specialty semiconductor fab**

March 01, 1995

Ticker Symbol: PRIA IDTI
Byline: Business Editors
Dateline: BILLERICA, Mass.
Time: 16:05 PT
Word Count: 378

BILLERICA, Mass.--(BUSINESS WIRE)--March 1, 1995--PRI Automation Inc. (NASDAQ:PRIA) said today that it has received a multi-year, $10 million order from Integrated Device Technology Inc., (NASDAQ:IDTI) for an automation system to be installed in IDT's new semiconductor fabrication facility being constructed in Hillsboro, Ore.

PRI Automation is the leading U.S. supplier of factory automation systems used by semiconductor manufacturing companies to optimize integrated circuit manufacturing.

Under the terms of the agreement, PRI will design and install an integrated transportation, storage and management system -- including monorails, stockers and control subsystems -- to move eight-inch silicon **wafers** through the front-end of the semiconductor manufacturing process at the IDT facility. This world-class facility will be the first eight-inch **wafer** fab built by IDT.

The contract calls for a phased approach to installation of the PRI equipment and related services beginning in mid-1995, according to Mitchell Tyson, president and chief operating officer of PRI Automation. This is the ninth full fab contract that PRI has been awarded in the last two years. The value of these contracts totals $100 million.

"PRI is pleased to be participating in IDT's expansion," said Tyson. "This venture will enable us to broaden our strategy of enriching the production facilities of both mid-size and specialty semiconductor producers."

Integrated Device Technology Inc. (IDT) designs, manufactures and markets CMOS VLSI integrated circuits (ICs) for a range of growth markets, including desktop computer, workstation/server, **data** communications and office automation. IDT offers products in four key areas: high-speed SRAMs, RISC microprocessors and high-performance logic. The company's product areas are synergistic and provide solutions that optimize the cost and performance of microprocessor-based systems. Headquartered in Santa Clara, CA, IDT employs approximately 2,850 people worldwide.

PRI Automation, headquartered in Billerica, MA, had its initial public offering on October 13, 1994. The company pioneered the design, development and manufacture of systems that automate the transport, storage and handling of silicon **wafers** used to make microprocessors, memory chips and other semiconductor components. PRI also provides system integration, factory simulation, project management and automation support services to its customers, which include many of the world's largest semiconductor companies.

sf

CONTACT: PRI Automation Inc.
John M. Chrisos, 508/670-4270, ext. 3032
Schwartz Communications Inc.
Pamela Hamilton or Michelle Goodall, 617/431-0770

KEYWORD: MASSACHUSETTS OREGON CALIFORNIA
INDUSTRY KEYWORD: COMPUTERS/ELECTRONICS COMED

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?ds

Set     Items   Description
S1         10   AU='WIESLER MORD':AU='WIESLER OREN'
S2         20   AU='MARIANO T':AU='MARIANO THOMAS R'
S3         27   S1:S2
S4          4   S3 AND (RETICLE? OR STOCKER?)
?show files
File 347:JAPIO Nov 1976-2004/Jan(Updated 040506)
         (c) 2004 JPO & JAPIO
File 350:Derwent WPIX 1963-2004/UD,UM &UP=200435
         (c) 2004  Thomson Derwent
File 348:EUROPEAN PATENTS 1978-2004/Jun W01
         (c) 2004 European Patent Office
File 349:PCT FULLTEXT 1979-2002/UB=20040603,UT=20040527
         (c) 2004 WIPO/Univentio
?
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?t s4/5/1-4

4/5/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014419547 **Image available**
WPI Acc No: 2002-240250/200229
XRPX Acc No: N02-185414
Reticle **management system that provides data storage and retrieval of data associated with each** reticle **and of movement and storage of** reticles **and their carriers**
Patent Assignee: PRI AUTOMATION INC (PRIA-N); MARIANO T (MARI-I); WIESLER O (WIES-I)
Inventor: **MARIANO T** ; **WIESLER O**
Number of Countries: 095 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
WO 200182055	A1	20011101	WO 2001US13349	A	20010425	200229 B
US 20010047222	A1	20011129	US 2000199453	P	20000425	200229
			US 2001842370	A	20010425	
AU 200159151	A	20011107	AU 200159151	A	20010425	200229

Priority Applications (No Type Date): US 2000199453 P 20000425; US 2001842370 A 20010425
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200182055	A1	E	39	G06F-007/00	

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZW

US 20010047222	A1		G06F-017/00	Provisional application US 2000199453
AU 200159151	A		G06F-007/00	Based on patent WO 200182055

Abstract (Basic): WO 200182055 A1
NOVELTY - Bays (101-107) each has a **stocker** (102,104,106,108) that contains lithographic **reticles** or semiconductor wafers and one or more processing stations (120-126,128-134,136-142,144-150) for processing the wafers. The bays are linked by a transport system (110) for the automatic transport of the wafers between the bays with the transport system and the processing stations.
DETAILED DESCRIPTION - AN INDEPENDENT CLAIM is included for a data managing apparatus.
USE - Management of **reticles** .
ADVANTAGE - Allowing user to access current data corresponding to various **reticles** .
DESCRIPTION OF DRAWING(S) - The drawing shows a wafer processing facility
Bays (101,103,105,107)
Stockers (102,104,106,108)
Processing stations (120-150)
Transport system (110)
pp; 39 DwgNo 1/6
Title Terms: **RETICLE** ; MANAGEMENT; SYSTEM; DATA; STORAGE; RETRIEVAL; DATA; ASSOCIATE; **RETICLE** ; MOVEMENT; STORAGE; **RETICLE** ; CARRY
Derwent Class: T01; U11
International Patent Class (Main): G06F-007/00; G06F-017/00
File Segment: EPI

4/5/2 (Item 1 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

01375230
RETICLE **MANAGEMENT SYSTEM**
SYSTEME DE GESTION DE RETICULES
PATENT ASSIGNEE:
Pri Automation, Inc., (2272440), 805 Middlesex Turnpike, Billerica, MA 01821-3986, (US), (Applicant designated States: all)
INVENTOR:
WIESLER, Oren , 7 York Road, Wayland, MA 01778, (US)
MARIANO, Thomas , 9 East Woodbine Drive, Londonderry, NH 03053, (US
PATENT (CC, No, Kind, Date): WO 2001082055 011101
APPLICATION (CC, No, Date): EP 2001932640 010425; WO 2001US13349 010425
PRIORITY (CC, No, Date): US 199453 P 000425
DESIGNATED STATES: AT; BE; CH; CY; DE; DK; ES; FI; FR; GB; GR; IE; IT; LI; LU; MC; NL; PT; SE; TR
EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI
INTERNATIONAL PATENT CLASS: G06F-007/00
CITED PATENTS (WO A): US 6078188 A ; US 6099598 A ; US 6188935 B1
LEGAL STATUS (Type, Pub Date, Kind, Text):
Application: 020102 A1 International application. (Art. 158(1))
Application: 020102 A1 International application entering European phase
Application: 030709 A1 International application. (Art. 158(1))
Appl Changed: 030709 A1 International application not entering European phase
Withdrawal: 030709 A1 Date application deemed withdrawn: 20021126
LANGUAGE (Publication,Procedural,Application): English; English; English

4/5/3 (Item 1 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

01080186
AUTOMATED MATERIAL HANDLING SYSTEM FOR SEMICONDUCTOR MANUFACTURING BASED ON A COMBINATION OF VERTICAL CAROUSELS AND OVERHEAD HOISTS
SYSTEME DE MANUTENTION AUTOMATISEE DE MATERIAUX DESTINE A LA MANUTENTION DE SEMI-CONDUCTEURS, UTILISANT UNE COMBINAISON DE CARROUSELS VERTICAUX ET DE PALANS AERIENS
Patent Applicant/Assignee:
BROOKS AUTOMATION INC, 15 Elizabeth Drive, Chelmsford, MA 01824, US, US (Residence), US (Nationality)
Inventor(s):
DOHERTY Brian J, 41 Cherry Brook Road, Weston, MA 02493, US,
MARIANO Thomas R , 9 E. Woodbine Drive, Londonderry, NH 03053, US,
SULLIVAN Robert P, 32 Fairmont Avenue, Wilmington, MA 01887, US
Legal Representative:
SCHURGIN Stanley M (et al) (agent), Weingarten, Schurgin, Gagnebin & Lebovici, LLP, 10 Post Office Square, Boston, MA 02109, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200401582 A1 20031231 (WO 0401582)
Application: WO 2003US8528 20030320 (PCT/WO US2003008528)
Priority Application: US 2002389993 20020619; US 2002417993 20021011
Designated States: CN JP KR SG
(EP) AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IT LU MC NL PT RO SE SI SK TR
Main International Patent Class: G06F-007/00
Publication Language: English
Filing Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 5368

English Abstract
A highly efficient Automated Material Handling System (AMHS) that allows

an overhead hoist transport vehicle to load and unload Work-In-Process (WIP) parts directly to/from one or more WIP storage units included in the system. The AMHS includes an overhead hoist transport subsystem and at least one vertical carousel **stocker** having a plurality of storage bins. The overhead hoist transport subsystem includes an overhead hoist transport vehicle traveling along a suspended track defining at least one predetermined route. The predetermined route passes over the vertical carousel **stocker** , which allows the overhead transport vehicle to access one or more WIP parts directly from one of the carousel storage bins. The selected carousel storage bin is positioned at the top of the vertical carousel **stocker** underneath the suspended track. Next, the overhead hoist transport vehicle is moved along the suspended track to a position above the selected carousel storage bin. The overhead hoist is then lowered parallel to the longitudinal axis of the vertical carousel **stocker** toward the selected storage bin.Finally, the overhead hoist is operated to pick the desired WIP lot directly from the carousel storage bin, or to place one or more WIP lots in the storage bin.

French Abstract

L'invention concerne un systeme de manutention automatisee de materiaux hautement efficace (AMHS) permettant a un vehicule de transport a palan aerien de directement charger et decharger des produits en cours de production vers ou a partir d'une ou de plusieurs unites de stockage de produits en cours de production utilises dans le systeme. Le systeme de manutention comprend un sous-systeme de transport a palan aerien et au moins dispositif de stockage equipe d'un carrousel vertical comportant une pluralite de cellules de stockage. Le sous-systeme de transport a palan aerien comprend un vehicule de transport a palan aerien se deplacant le long d'un circuit aerien decrivant au moins un trajet predetermine. Le trajet predetermine passe par dessus le dispositif de stockage vertical, ce qui permet au vehicule de transport aerien d'acceder directement a un ou plusieurs des produits en cours de production depuis une des cellules de stockage du carrousel. La cellule de stockage selectionnee du carrousel est placee au sommet du dispositif de stockage equipe du carrousel vertical, sous le circuit aerien. Ensuite, le vehicule de transport a palan aerien est deplace le long du circuit aerien vers une position situee au-dessus de la cellule de stockage selectionnee du carrousel. Le palan aerien est par la suite abaisse parallelement a l'axe longitudinal du dispositif de stockage equipe du carrousel vertical, vers la cellule de stockage selectionnee. Finalement, le palan aerien est utilise pour saisir le lot en cours de production directement dans la cellule de stockage du carrousel ou pour placer un ou plusieurs lots en cours de production dans la cellule de stockage.

Legal Status (Type, Date, Text)
Publication 20031231 A1 With international search report.

4/5/4 (Item 2 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00848452 **Image available**
RETICLE **MANAGEMENT SYSTEM**
SYSTEME DE GESTION DE RETICULES
Patent Applicant/Assignee:
PRI AUTOMATION INC, 805 Middlesex Turnpike, Billerica, MA 01821-3896, US, US (Residence), US (Nationality)
Inventor(s):
WIESLER Oren , 7 York Road, Wayland, MA 01778, US,
MARIANO Thomas , 9 East Woodbine Drive, Londonderry, NH 03053, US
Legal Representative:
HJORTH Beverly E (et al) (agent), Weingarten, Schurgin, Gagnebin & Hayes, LLP, Ten Post Office Square, Boston, MA 02109, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200182055 A1 20011101 (WO 0182055)

Application: WO 2001US13349 20010425 (PCT/WO US0113349)
Priority Application: US 2000199453 20000425
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU
CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR
KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE
SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Main International Patent Class: G06F-007/00
Publication Language: English
Filing Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 5987

English Abstract
A **reticle** management system (100) is disclosed that provides data storage and retrieval of data associated with each **reticle** , **reticle** carrier, and certain system attributes and also for the efficient movement and storage of **reticles** and **reticle** carriers. The **reticle** management system includes a **reticle** management controller, a central **reticle** database, and one or more **reticle stockers** (102,104,106,108) that include a **stocker** controller, a **stocker** database, and a **stocker** unit.

French Abstract
L'invention concerne un systeme de gestion de reticules (100) permettant de memoriser et d'extraire des donnees associees a chaque reticule, a chaque support de reticule et a certains attributs de systeme et permettant egalement de deplacer et de memoriser efficacement des reticules et des supports de reticule. Ce systeme de gestion de reticules comporte un controleur de gestion de reticules, une base de donnees centrale de reticules et un ou plusieurs stockeurs de reticules (102,104,106,108) comportant un controleur de stockage, une base de donnees de stockage et une unite de stockage.

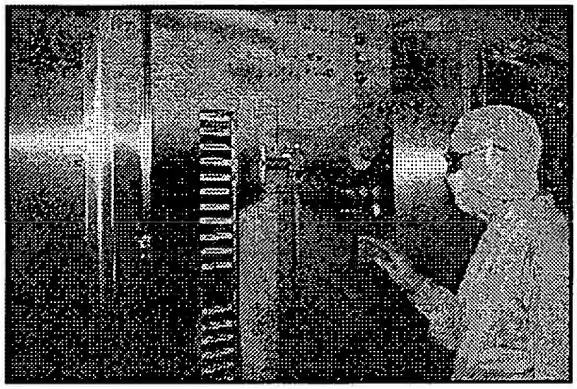
Legal Status (Type, Date, Text)
Publication 20011101 A1 With international search report.
Examination 20020328 Request for preliminary examination prior to end of 19th month from priority date

?

Semiconductor Equipment Assessment
Linking European Equipment Suppliers with Global Users

esprit

Project RETIMATIC



DMS Automatic Reticle Stocker

Comments from...

ALCATEL MIETEC equipment site (node)

DMS equipment supplier

Other partners

TEMIC

Assessment of the performance of a reticle stocker with integrated database and the productivity gain obtained in a submicron ASIC waferfab

■ *Objectives* ■

■To assess the equipment performance of the carousel reticle stocker with an integrated reticle database and barcode reader■

■To evaluate the productivity gain obtained by using this stocker in a submicron waferfab for ASIC fabrication■

■To integrate the reticle stocker with the waferfab CIM system and evaluate the extra efficiency gain■

Evaluation period - 1 April 1996 to 28 February 1997

SEA Projects | SEA Home Page

Assessment Of Potential Gains In Productivity Due To Proactive Reticle Management Using Discrete Event Simulation (Make Corrections)

Proceedings of the 1999 Winter Simulation Conference P. A. Farrington, H. B....
Winter Simulation Conference

Abstract: Photolithography is often the constraining equipment in semiconductor wafer fabrication plants due to the number of times the product must process through it. Modern day photolithography is performed on a cluster tool that is a combination of a stepper and track. It is obvious that the combined availability of the cluster tool is critical to throughput, but what is not so obvious is the throughput restriction from a secondary constraint known as a reticle. Every layer of a product needs a... (Update)


```
@inproceedings{ park99assessment,
    author = "Sungmin Park and John W. Fowler and Matt Carlyle and Matt Hickie",
    title = "Assessment of potential gains in productivity due to proactive reticle
    booktitle = "Winter Simulation Conference",
    pages = "856-864",
    year = "1999",
    url = "citeseer.ist.psu.edu/406577.html" }
```

Citations (may not include all citations):
10 North River Press (context) - Goldratt, Cox - 1986

Reticle Management Study for MiCRUS, Inc. (Make Corrections)

Cornell University Micrus School Of Operations Research And Industrial Engineering College Of Engineering ...

Abstract: The objective of this project is to analyze and recommend an appropriate system for reticle management in the photolithography area at MiCRUS. (Update)